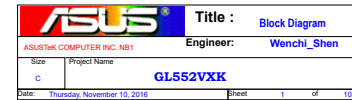


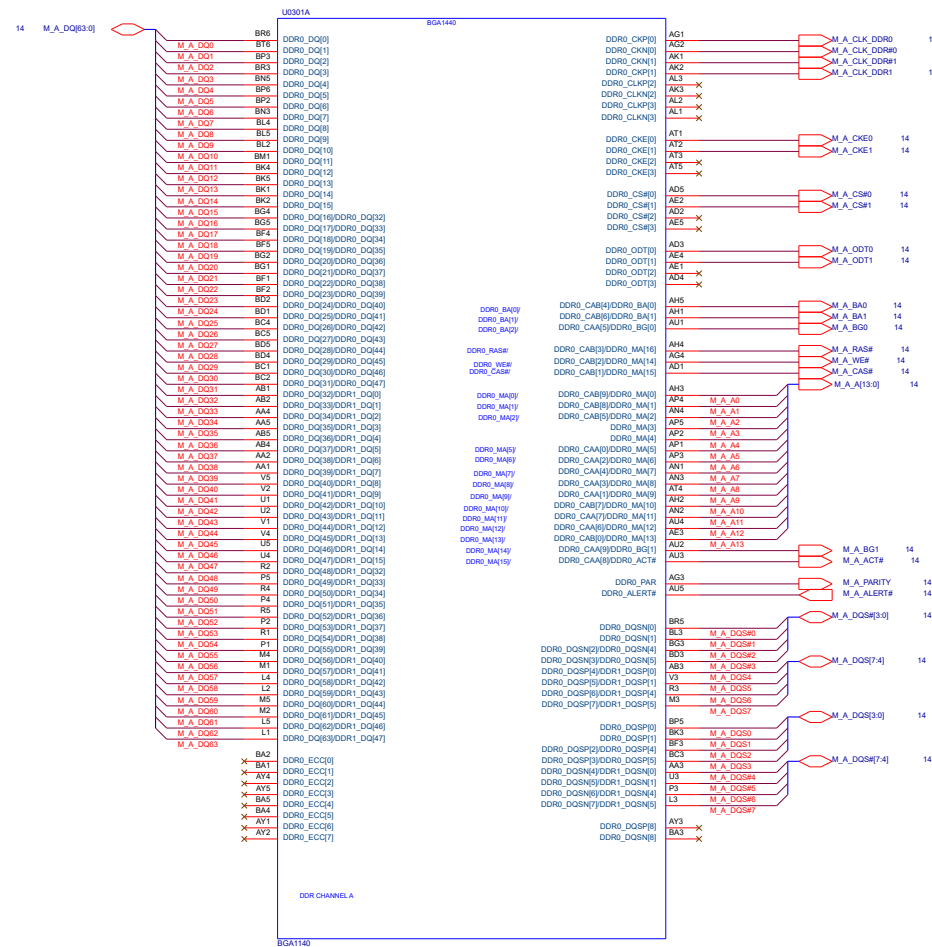
Kaby lake Platform

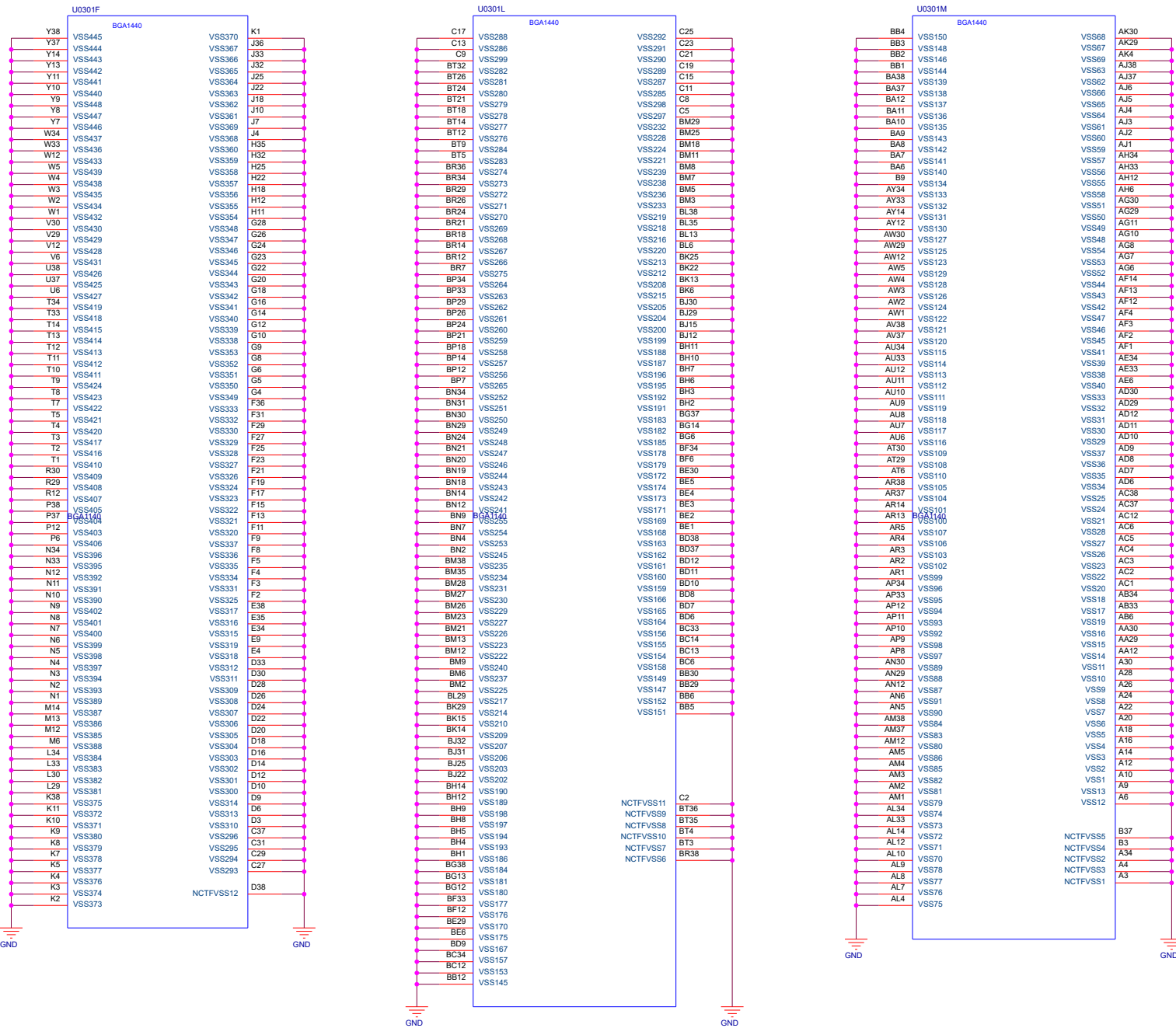


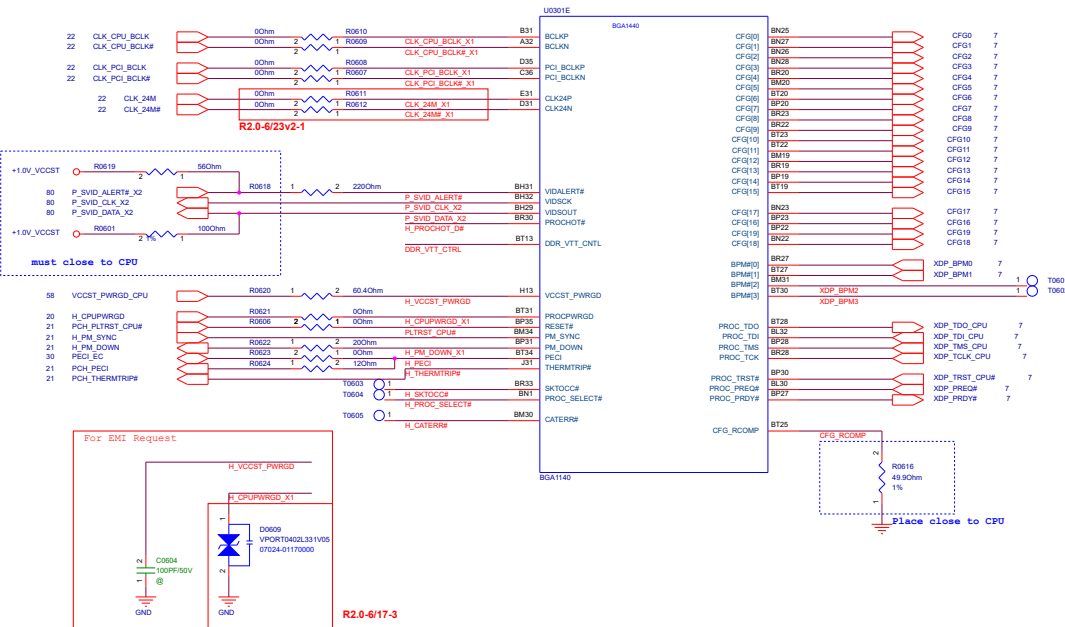
Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power
EXT_A0	GPIO0	RAWLW0	RC_100	PD 100	+100
EXT_A1	LATCH	RAWLW1			
EXT_A2	RAWLW2	RAWLW2	LATCH_A02		+100
EXT_A3	LATCH	RAWLW3	LATCH_A03		+100
EXT_A4	LATCH	RAWLW4	LATCH_A04		+100
EXT_A5	LATCH	RAWLW5	LATCH_A05		+100
EXT_A6	RAWLW6	RAWLW6	INT_100W		+100
EXT_A7	RAWLW7	RAWLW7	INT_100W		+100
EXT_A8	GPIO08	RAWLW8	RC_100W	PD 100W	+100
EXT_A9	GPIO9	RAWLW9	RC_100W120W_93		+100
EXT_A10	GPIO10	RAWLW10	RC_100W120W_10		+100
EXT_A11	GPIO11	RAWLW11	RC_100W120W_11		+100
EXT_A12	GPIO12	RAWLW12	RC_100W120W_12		+100
EXT_A13	GPIO13	RAWLW13	RC_100W120W_13		+100
EXT_A14	GPIO14	RAWLW14	RC_100W120W_14		+100
EXT_A15	GPIO15	RAWLW15	RC_100W120W_15		+100
EXT_A16	GPIO16	RAWLW16	RC_100W120W_16		+100
EXT_A17	GPIO17	RAWLW17	RC_100W120W_17		+100
EXT_A18	GPIO18	RAWLW18	RC_100W120W_18		+100
EXT_A19	GPIO19	RAWLW19	RC_100W120W_19		+100
EXT_A20	GPIO20	RAWLW20	RC_100W120W_20		+100
EXT_A21	GPIO21	RAWLW21	RC_100W120W_21		+100
EXT_A22	GPIO22	RAWLW22	RC_100W120W_22		+100
EXT_A23	GPIO23	RAWLW23	RC_100W120W_23		+100
EXT_A24	GPIO24	RAWLW24	RC_100W120W_24		+100
EXT_A25	GPIO25	RAWLW25	RC_100W120W_25		+100
EXT_A26	GPIO26	RAWLW26	RC_100W120W_26		+100
EXT_A27	GPIO27	RAWLW27	RC_100W120W_27		+100
EXT_A28	GPIO28	RAWLW28	RC_100W120W_28		+100
EXT_A29	GPIO29	RAWLW29	RC_100W120W_29		+100
EXT_A30	GPIO30	RAWLW30	RC_100W120W_30		+100
EXT_A31	GPIO31	RAWLW31	RC_100W120W_31		+100
EXT_A32	GPIO32	RAWLW32	RC_100W120W_32		+100
EXT_A33	GPIO33	RAWLW33	RC_100W120W_33		+100
EXT_A34	GPIO34	RAWLW34	RC_100W120W_34		+100
EXT_A35	GPIO35	RAWLW35	RC_100W120W_35		+100
EXT_A36	GPIO36	RAWLW36	RC_100W120W_36		+100
EXT_A37	GPIO37	RAWLW37	RC_100W120W_37		+100
EXT_A38	GPIO38	RAWLW38	RC_100W120W_38		+100
EXT_A39	GPIO39	RAWLW39	RC_100W120W_39		+100
EXT_A40	GPIO40	RAWLW40	RC_100W120W_40		+100
EXT_A41	GPIO41	RAWLW41	RC_100W120W_41		+100
EXT_A42	GPIO42	RAWLW42	RC_100W120W_42		+100
EXT_A43	GPIO43	RAWLW43	RC_100W120W_43		+100
EXT_A44	GPIO44	RAWLW44	RC_100W120W_44		+100
EXT_A45	GPIO45	RAWLW45	RC_100W120W_45		+100
EXT_A46	GPIO46	RAWLW46	RC_100W120W_46		+100
EXT_A47	GPIO47	RAWLW47	RC_100W120W_47		+100
EXT_A48	GPIO48	RAWLW48	RC_100W120W_48		+100
EXT_A49	GPIO49	RAWLW49	RC_100W120W_49		+100
EXT_A50	GPIO50	RAWLW50	RC_100W120W_50		+100
EXT_A51	GPIO51	RAWLW51	RC_100W120W_51		+100
EXT_A52	GPIO52	RAWLW52	RC_100W120W_52		+100
EXT_A53	GPIO53	RAWLW53	RC_100W120W_53		+100
EXT_A54	GPIO54	RAWLW54	RC_100W120W_54		+100
EXT_A55	GPIO55	RAWLW55	RC_100W120W_55		+100
EXT_A56	GPIO56	RAWLW56	RC_100W120W_56		+100
EXT_A57	GPIO57	RAWLW57	RC_100W120W_57		+100
EXT_A58	GPIO58	RAWLW58	RC_100W120W_58		+100
EXT_A59	GPIO59	RAWLW59	RC_100W120W_59		+100
EXT_A60	GPIO60	RAWLW60	RC_100W120W_60		+100
EXT_A61	GPIO61	RAWLW61	RC_100W120W_61		+100
EXT_A62	GPIO62	RAWLW62	RC_100W120W_62		+100
EXT_A63	GPIO63	RAWLW63	RC_100W120W_63		+100
EXT_A64	GPIO64	RAWLW64	RC_100W120W_64		+100
EXT_A65	GPIO65	RAWLW65	RC_100W120W_65		+100
EXT_A66	GPIO66	RAWLW66	RC_100W120W_66		+100
EXT_A67	GPIO67	RAWLW67	RC_100W120W_67		+100
EXT_A68	GPIO68	RAWLW68	RC_100W120W_68		+100
EXT_A69	GPIO69	RAWLW69	RC_100W120W_69		+100
EXT_A70	GPIO70	RAWLW70	RC_100W120W_70		+100
EXT_A71	GPIO71	RAWLW71	RC_100W120W_71		+100
EXT_A72	GPIO72	RAWLW72	RC_100W120W_72		+100
EXT_A73	GPIO73	RAWLW73	RC_100W120W_73		+100
EXT_A74	GPIO74	RAWLW74	RC_100W120W_74		+100
EXT_A75	GPIO75	RAWLW75	RC_100W120W_75		+100
EXT_A76	GPIO76	RAWLW76	RC_100W120W_76		+100
EXT_A77	GPIO77	RAWLW77	RC_100W120W_77		+100
EXT_A78	GPIO78	RAWLW78	RC_100W120W_78		+100
EXT_A79	GPIO79	RAWLW79	RC_100W120W_79		+100
EXT_A80	GPIO80	RAWLW80	RC_100W120W_80		+100
EXT_A81	GPIO81	RAWLW81	RC_100W120W_81		+100
EXT_A82	GPIO82	RAWLW82	RC_100W120W_82		+100
EXT_A83	GPIO83	RAWLW83	RC_100W120W_83		+100
EXT_A84	GPIO84	RAWLW84	RC_100W120W_84		+100
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EXT_A86	GPIO86	RAWLW86	RC_100W120W_86		+100
EXT_A87	GPIO87	RAWLW87	RC_100W120W_87		+100
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EXT_A89	GPIO89	RAWLW89	RC_100W120W_89		+100
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EXT_A91	GPIO91	RAWLW91	RC_100W120W_91		+100
EXT_A92	GPIO92	RAWLW92	RC_100W120W_92		+100
EXT_A93	GPIO93	RAWLW93	RC_100W120W_93		+100
EXT_A94	GPIO94	RAWLW94	RC_100W120W_94		+100
EXT_A95	GPIO95	RAWLW95	RC_100W120W_95		+100
EXT_A96	GPIO96	RAWLW96	RC_100W120W_96		+100
EXT_A97	GPIO97	RAWLW97	RC_100W120W_97		+100
EXT_A98	GPIO98	RAWLW98	RC_100W120W_98		+100
EXT_A99	GPIO99	RAWLW99	RC_100W120W_99		+100
EXT_A100	GPIO100	RAWLW100	RC_100W120W_100		+100
EXT_A101	GPIO101	RAWLW101	RC_100W120W_101		+100
EXT_A102	GPIO102	RAWLW102	RC_100W120W_102		+100
EXT_A103	GPIO103	RAWLW103	RC_100W120W_103		+100
EXT_A104	GPIO104	RAWLW104	RC_100W120W_104		+100
EXT_A105	GPIO105	RAWLW105	RC_100W120W_105		+100
EXT_A106	GPIO106	RAWLW106	RC_100W120W_106		+100
EXT_A107	GPIO107	RAWLW107	RC_100W120W_107		+100
EXT_A108	GPIO108	RAWLW108	RC_100W120W_108		+100
EXT_A109	GPIO109	RAWLW109	RC_100W120W_109		+100
EXT_A110	GPIO110	RAWLW110	RC_100W120W_110		+100
EXT_A111	GPIO111	RAWLW111	RC_100W120W_111		+100
EXT_A112	GPIO112	RAWLW112	RC_100W120W_112		+100
EXT_A113	GPIO113	RAWLW113	RC_100W120W_113		+100
EXT_A114	GPIO114	RAWLW114	RC_100W120W_114		+100
EXT_A115	GPIO115	RAWLW115	RC_100W120W_115		+100
EXT_A116	GPIO116	RAWLW116	RC_100W120W_116		+100
EXT_A117	GPIO117	RAWLW117	RC_100W120W_117		+100
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EXT_A122	GPIO122	RAWLW122	RC_100W120W_122		+100
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EXT_A126	GPIO126	RAWLW126	RC_100W120W_126		+100
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EXT_A128	GPIO128	RAWLW128	RC_100W120W_128		+100
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EXT_A130	GPIO130	RAWLW130	RC_100W120W_130		+100
EXT_A131	GPIO131	RAWLW131	RC_100W120W_131		+100
EXT_A132	GPIO132	RAWLW132	RC_100W120W_132		+100
EXT_A133	GPIO133	RAWLW133	RC_100W120W_133		+100
EXT_A134	GPIO134	RAWLW134	RC_100W120W_134		+100
EXT_A135	GPIO135	RAWLW135	RC_100W120W_135		+100
EXT_A136	GPIO136	RAWLW136	RC_100W120W_136		+100
EXT_A137	GPIO137	RAWLW137	RC_100W120W_137		+100
EXT_A138	GPIO138	RAWLW138	RC_100W120W_138		+100
EXT_A139	GPIO139	RAWLW139	RC_100W120W_139		+100
EXT_A140	GPIO140	RAWLW140	RC_100W120W_140		+100
EXT_A141	GPIO141	RAWLW141	RC_100W120W_141		+100
EXT_A142	GPIO142	RAWLW142	RC_100W120W_142		+100
EXT_A143	GPIO143	RAWLW143	RC_100W120W_143		+100
EXT_A144	GPIO144	RAWLW144	RC_100W120W_144		+100
EXT_A145	GPIO145	RAWLW145	RC_100W120W_145		+100
EXT_A146	GPIO146	RAWLW146	RC_100W120W_146		+100
EXT_A147	GPIO147	RAWLW147	RC_100W120W_147		+100
EXT_A148	GPIO148	RAWLW148	RC_100W120W_148		+100
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EXT_A151	GPIO151	RAWLW151	RC_100W120W_151		+100
EXT_A152	GPIO152	RAWLW152	RC_100W120W_152		+100
EXT_A153	GPIO153	RAWLW153	RC_100W120W_153		+100
EXT_A154	GPIO154	RAWLW154	RC_100W120W_154		+100
EXT_A155	GPIO155	RAWLW155	RC_100W120W_155		+100
EXT_A156	GPIO156	RAWLW156	RC_100W120W_156		+100
EXT_A157	GPIO157	RAWLW157	RC_100W120W_157		+100
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EXT_A159	GPIO159	RAWLW159	RC_100W120W_159		+100
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EXT_A161	GPIO161	RAWLW161	RC_100W120W_161		+100
EXT_A162	GPIO162	RAWLW162	RC_100W120W_162		+100
EXT_A163	GPIO163	RAWLW163	RC_100W120W_163		+100
EXT_A164	GPIO164	RAWLW164	RC_100W120W_164		+100
EXT_A165	GPIO165	RAWLW165	RC_100W120W_165		+100
EXT_A166	GPIO166	RAWLW166	RC_100W120W_166		+100
EXT_A167	GPIO167	RAWLW167	RC_100W120W_167		+100
EXT_A168	GPIO168	RAWLW168	RC_100W120W_168		+100
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EXT_A170	GPIO170	RAWLW170	RC_100W120W_170		+100
EXT_A171	GPIO171	RAWLW171	RC_100W120W_171		+100
EXT_A172	GPIO172	RAWLW172	RC_100W120W_172		+100
EXT_A173	GPIO173	RAWLW173	RC_100W120W_173		+100
EXT_A174	GPIO174	RAWLW174	RC_100W120W_174		+100
EXT_A175	GPIO175	RAWLW175	RC_100W120W_175		+100
EXT_A176	GPIO176	RAWLW176	RC_100W120W_176		+100
EXT_A177	GPIO177	RAWLW177	RC_100W120W_177		+100
EXT_A178	GPIO178	RAWLW178	RC_100W120W_178		+100
EXT_A179	GPIO179	RAWLW179	RC_100W120W_179		+100
EXT_A180	GPIO180	RAWLW180	RC_100W120W_180		+100
EXT_A181	GPIO181	RAWLW181	RC_100W120W_181		+100
EXT_A182	GPIO182	RAWLW182	RC_100W120W_182		+100
EXT_A183	GPIO183	RAWLW183	RC_100W120W_183		+100
EXT_A184	GPIO184	RAWLW184	RC_100W120W_184		+100
EXT_A185	GPIO185	RAWLW185	RC_100W120W_185		+100
EXT_A186	GPIO186	RAWLW186	RC_100W120W_186		+100
EXT_A187	GPIO187	RAWLW187	RC_100W120W_187		+100
EXT_A188	GPIO188	RAWLW188	RC_100W120W_188		+100
EXT_A189	GPIO189	RAWLW189	RC_100W120W_189		+100
EXT_A190	GPIO190	RAWLW190	RC_100W120W_190		+100
EXT_A191	GPIO191	RAWLW191	RC_100W120W_191		+100
EXT_A192	GPIO192	RAWLW192	RC_100W120W_192		+100
EXT_A193	GPIO193	RAWLW193	RC_100W120W_193		+100
EXT_A194	GPIO194	RAWLW194	RC_100W120W_194		+100
EXT_A195	GPIO195</				

R2.0-6/9-7

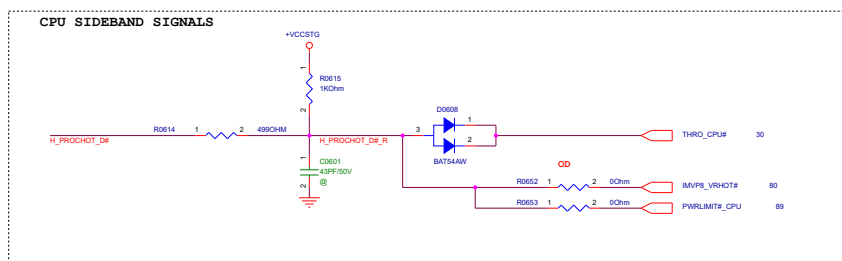
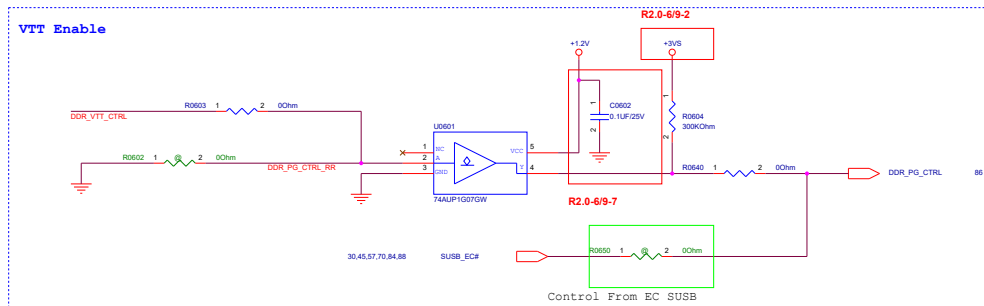
Memory Channel A



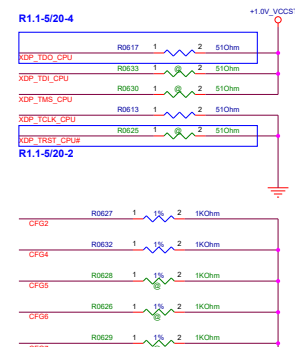




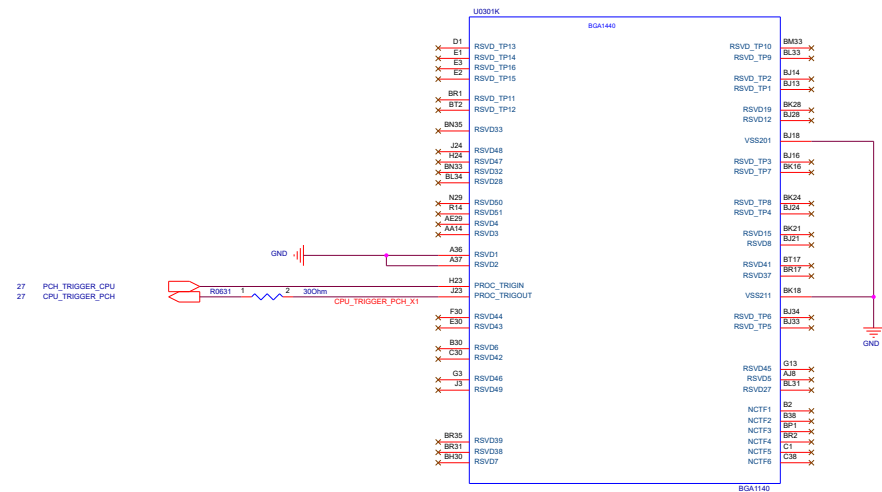
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

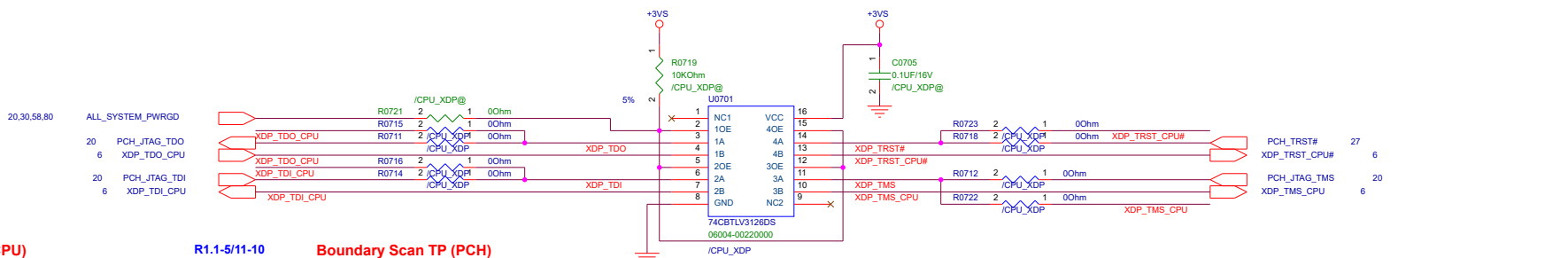
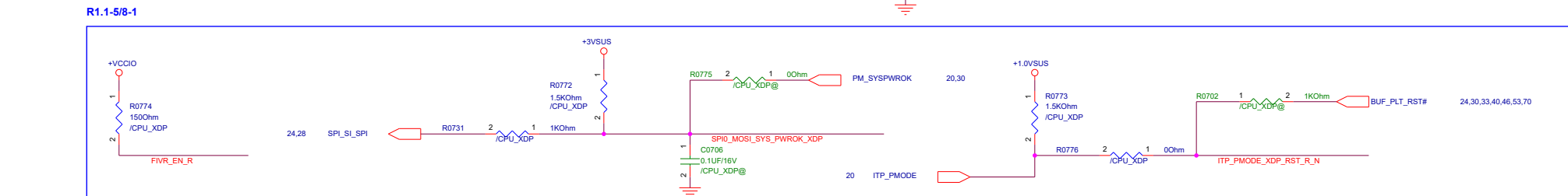
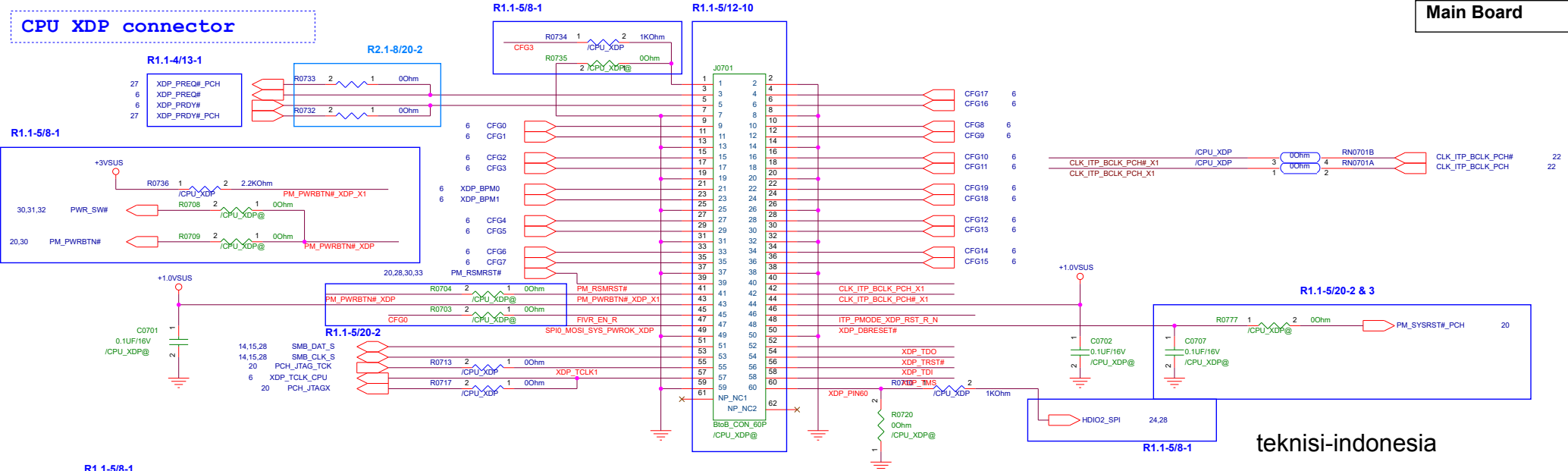


CFG Straps



<p>CFG Straps for Processor</p> <p>ref: Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121</p>
<p>CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted</p> <ul style="list-style-type: none"> - 1 : (Default) Normal Operation; No stall - 0 : Stall
<p>CFG[1] : Reserved Configuration Lane</p> <p>Reserved Configuration Lane</p>
<p>CFG[2] : PCI Express* Static x16 Lane Numbering Reversal</p> <ul style="list-style-type: none"> - 1 : (Default) Normal Operation - 0 : Lane Numbers Reversed
<p>CFG[3] : Reserved configuration lanes</p> <p>Reserved Configuration Lane</p>
<p>CFG[4] : eDP Enable</p> <ul style="list-style-type: none"> - 1 : Disabled - 0 : Enabled
<p>CFG[6:5] : PCI Express* Bifurcation</p> <ul style="list-style-type: none"> - 00 : 1 x8 , 2 x4 PCI Express* - 01 : Reserved - 10 : 2 x8 PCI Express* - 11 : 1 x16 PCI Express*
<p>CFG[7] : PEG Training</p> <ul style="list-style-type: none"> - 1 : (Default) PEG Train Immediately Following RESET# de-assertion - 0 : PEG Wait for BIOS for Training
<p>CFG[19:8] : Reserved Configuration Lanes</p> <p>Reserved Configuration Lanes</p>
<p>Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121 Richard 2014T209</p>

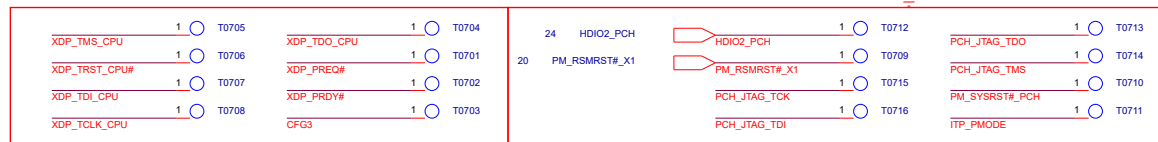




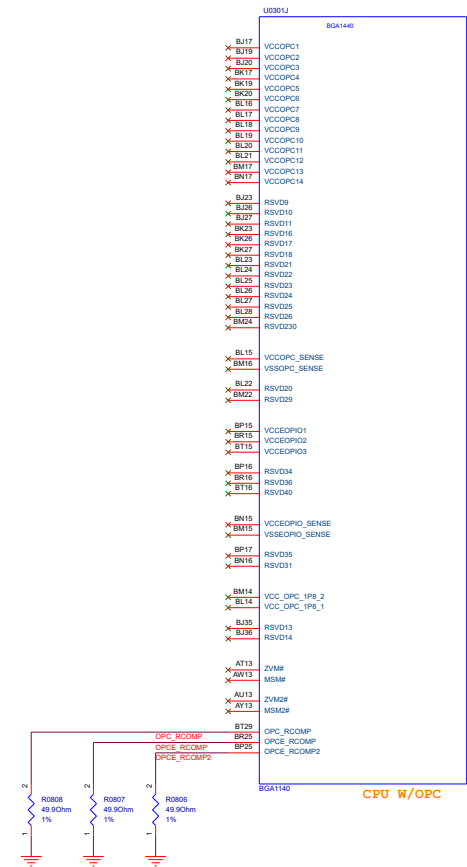
Boundary Scan TP (CPU)

R1.1-5/11-10

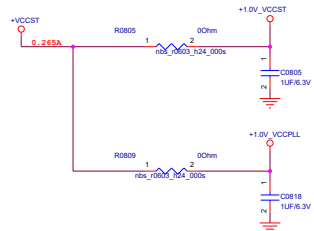
Boundary Scan TP (PCH)



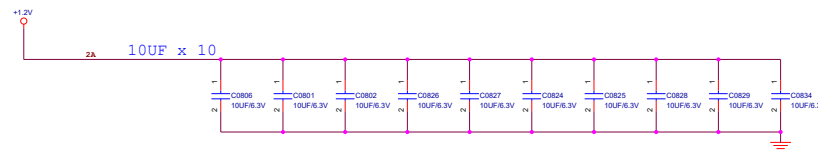
OPC Power Rails



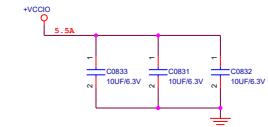
CPU W/OPC

+1.0V_VCCST/+1.0V_VCCPLL
DECAPS Place Back Side (TOP)

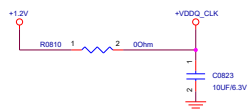
+VDDQ DECAPS Place Back Side (TOP)



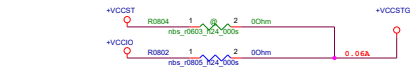
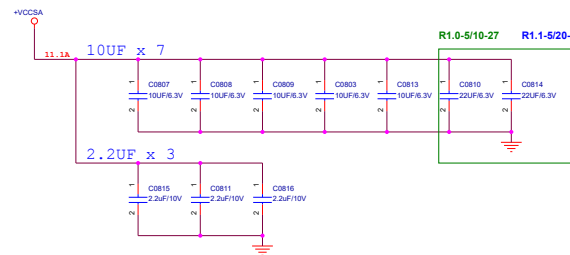
+VCCIO DECAPS Place Back Side (TOP)



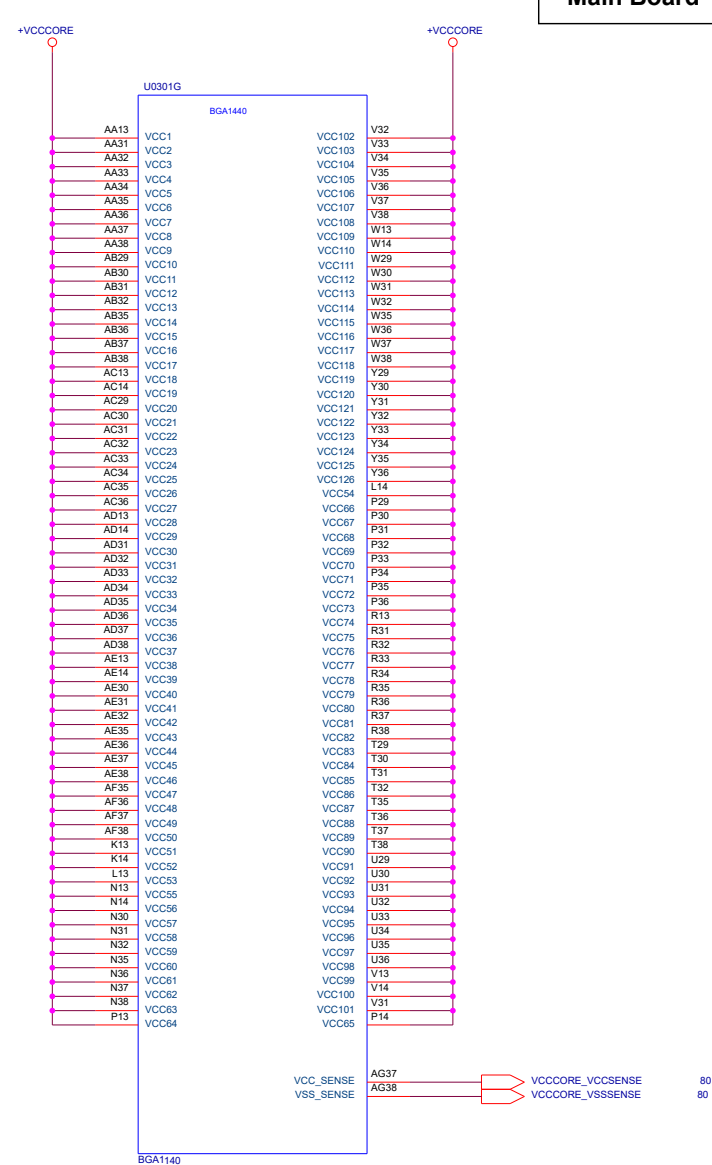
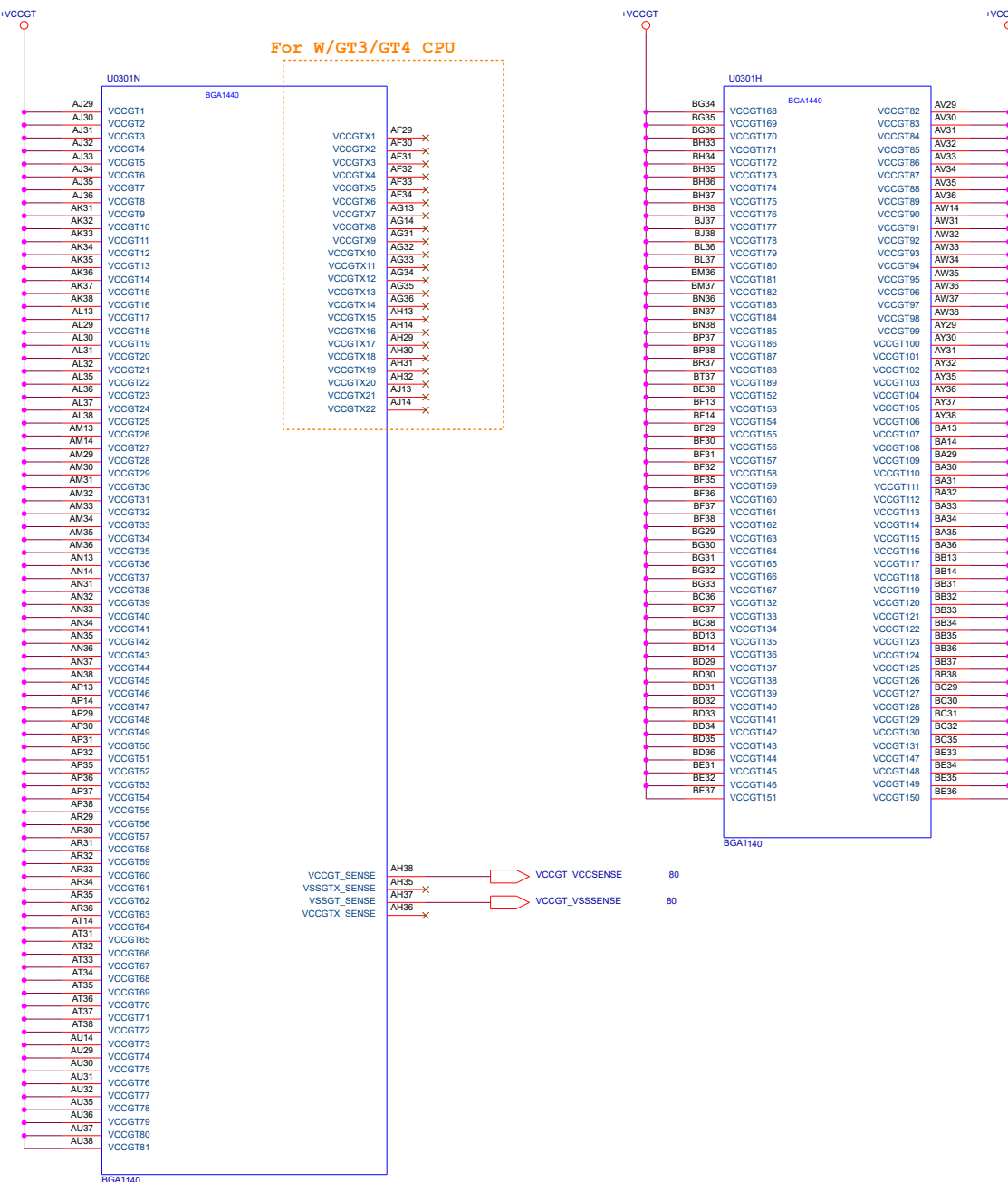
+VDDQ_CLK DECAPS Place Back Side (TOP)



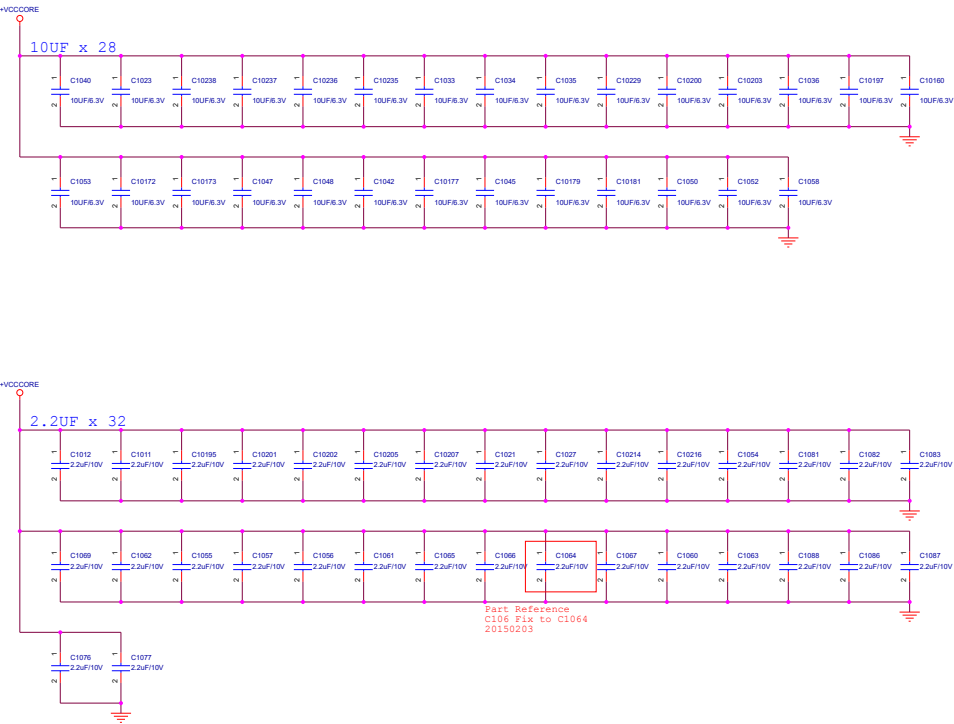
+VCCSA DECAPS Place Back Side (TOP)



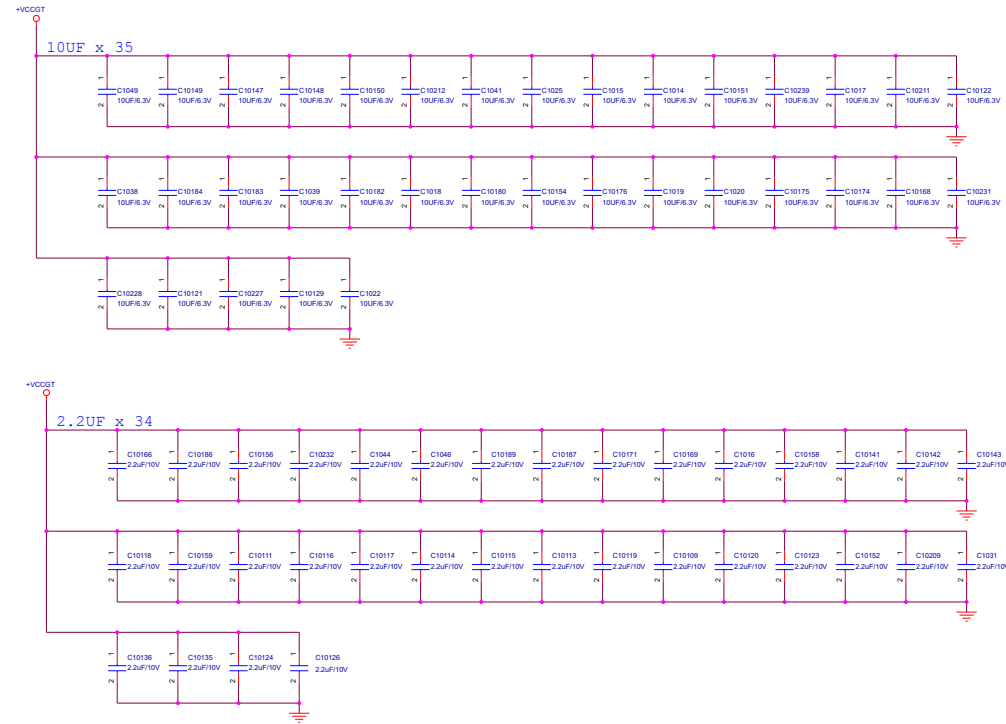
Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)



+VCCORE DECAPS Place Back Side (TOP)



+VCCGT DECAPS Place Back Side (TOP)





Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0



Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0



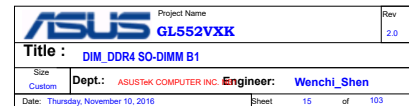
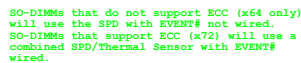
Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0

12002-00080400
DDR4 DIMM 260P 8H REV





Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK teknisi-indonesia	2.0

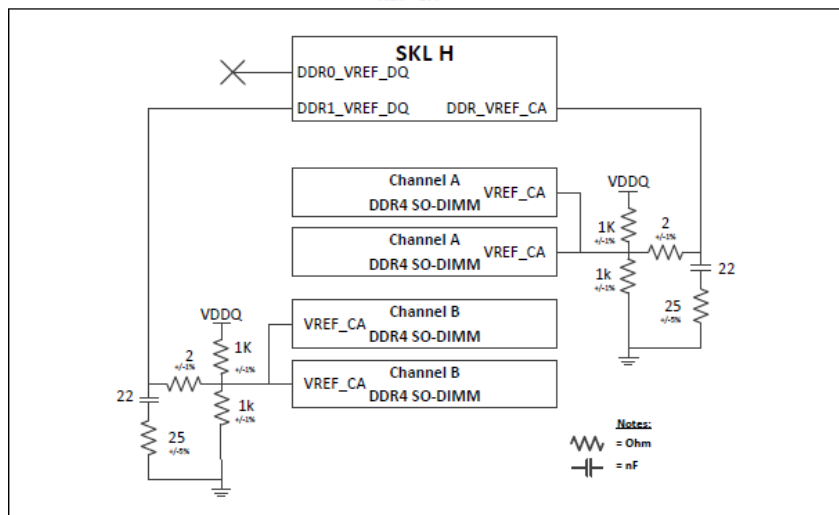


Title : NB_****

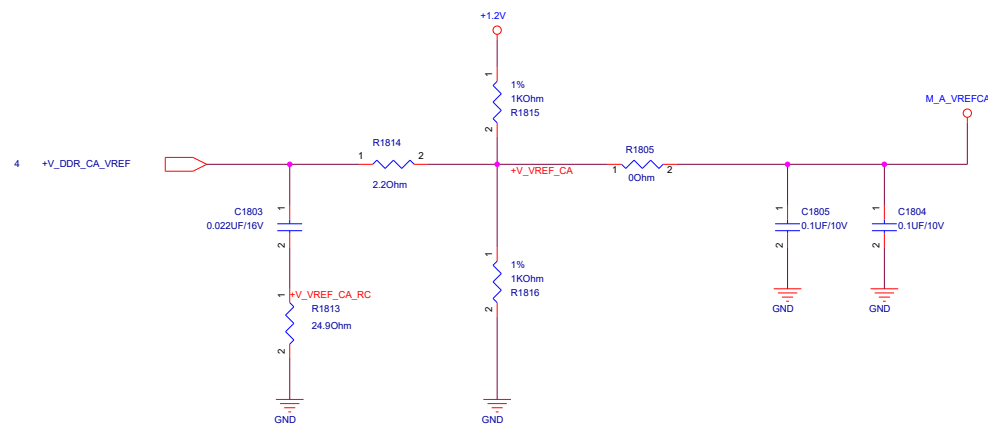
ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

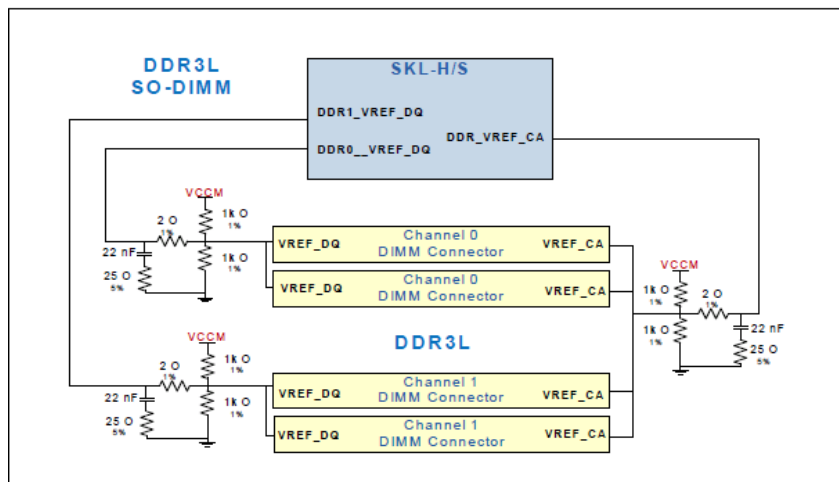
Size	Project Name	Rev
A	GL552VXK	2.0

SKL H DDR4/DDR4-RS SO-DIMM V_{REF_CA} Overview

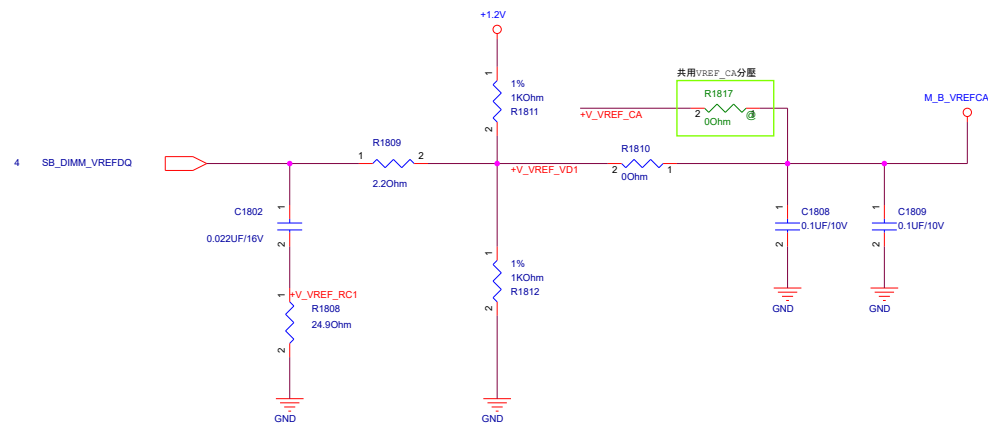
SO-DIMM0 Vref



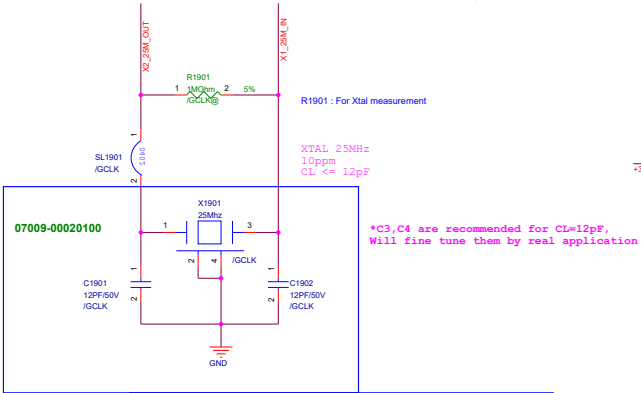
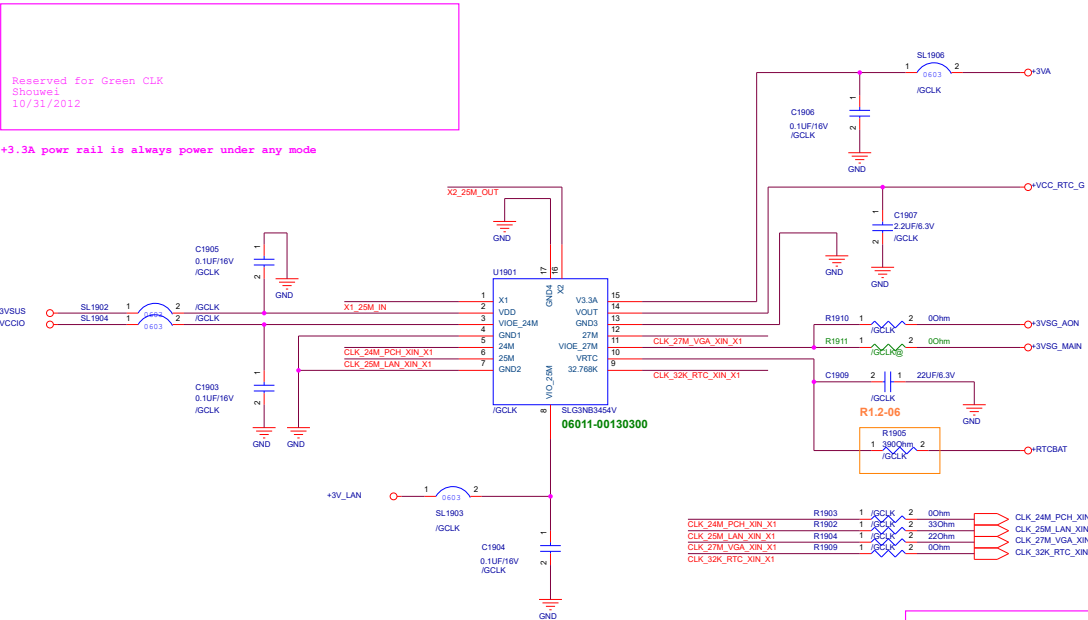
SKL H and SKL S DDR3L SODIMM VREF Overview



SO-DIMM1 Vref



Silego Green CLK



R1.1-4/13-5

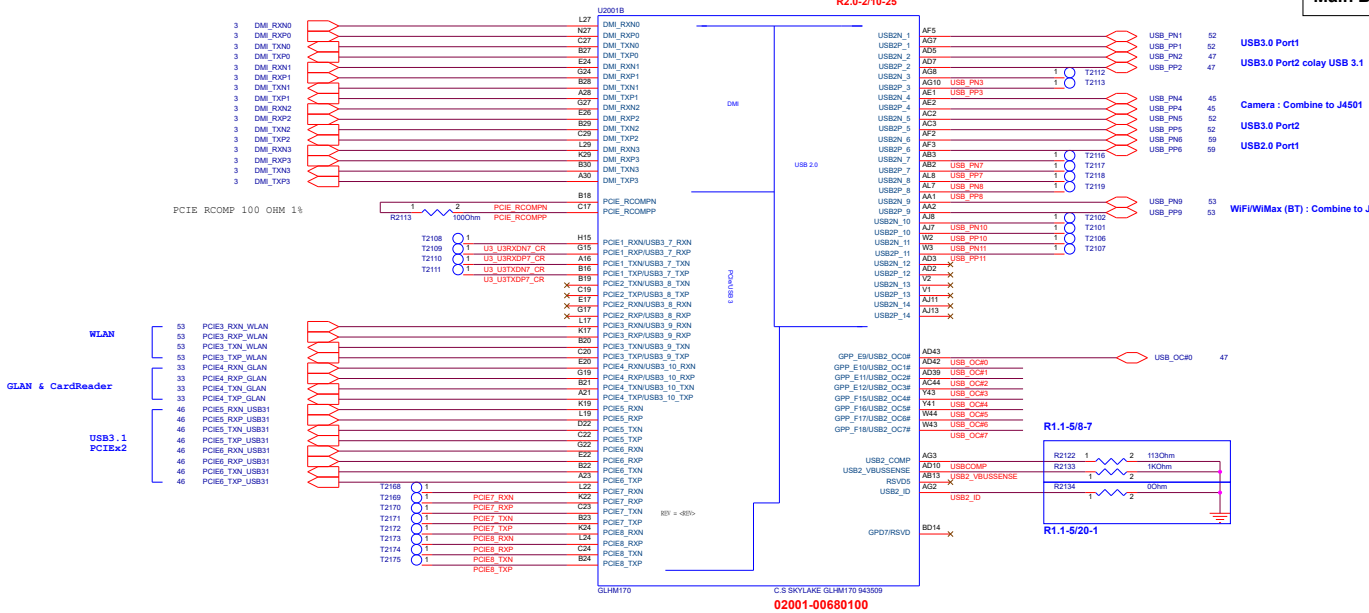
X1901: 25MHZ +/-20ppm/10pF (3225)
1st: P/N:07009-00020700 HOSONIC/E3FB25.0000F10E22
2nd: P/N:07009-00020800 TXC/7V25000036
3rd: P/N:07009-00020100 EPSON/FA-238G

R1.1-4/13-5

Main Board

GL552VXK PCIE Function define
Kabylake HM175

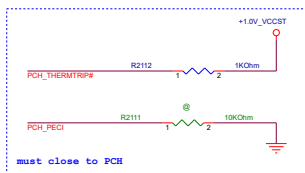
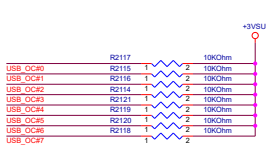
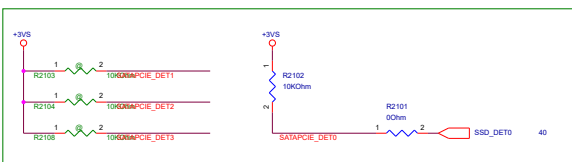
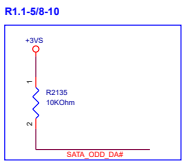
HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)		SRC0
01	USB#001	USB3_IO	
02	USB#002 / SSIC#01	USB3.0 IO colay USB3.1	
03	USB#003 / SSIC#02	USB3.0 IO colay USB3.1	
04	USB#004		
05	USB#005	USB3_IO	
06	USB#006		
07	USB#007 / PCIE#01		
08	USB#008 / PCIE#02		
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN & CardReader	SRC4
11	PCIE#05 / GBE		
12	PCIE#06	USB 3.1	SRC5
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE		
16	PCIE#10 / SATA#1	PCIE*4 / SATA SSD or Optane	SRC6
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE	Reserve for Optane	
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2	HDD	
22	PCIE#16 / SATA#3	ODD	
23			
24			
25			
26			

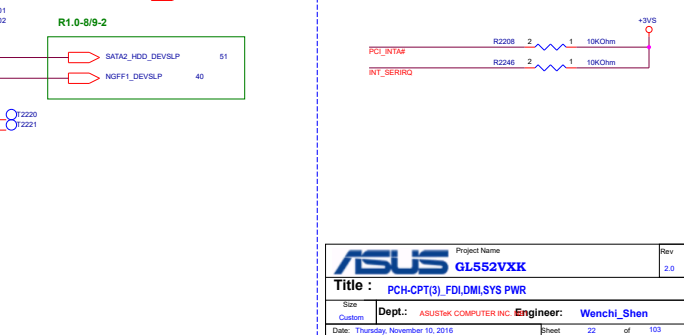
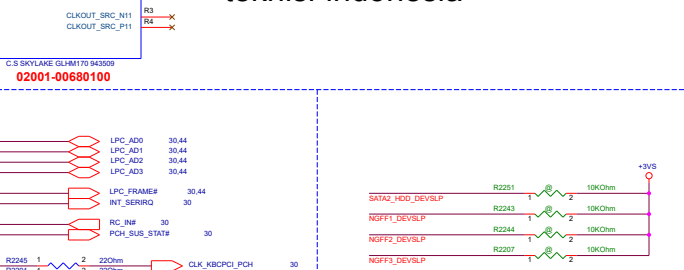
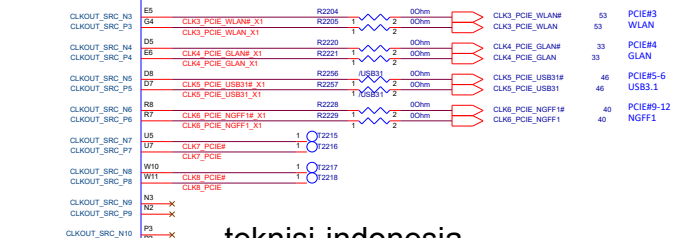
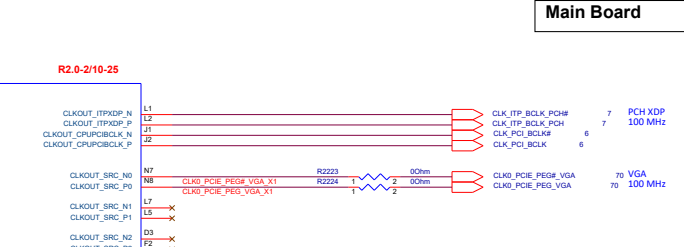
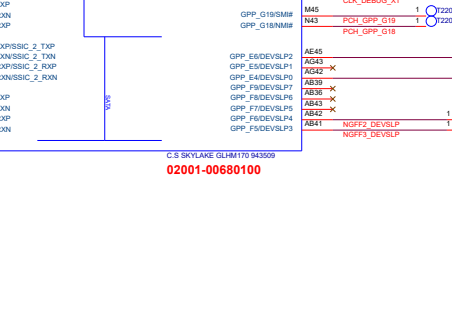
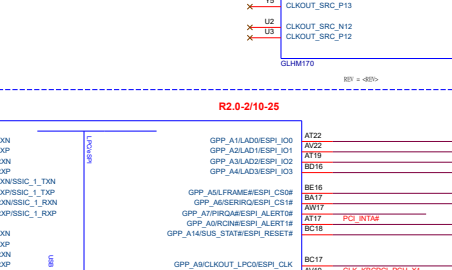
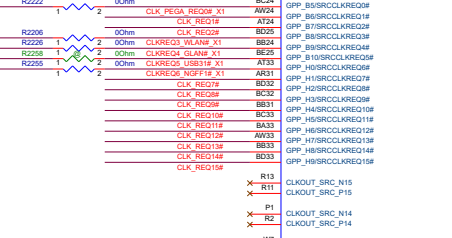
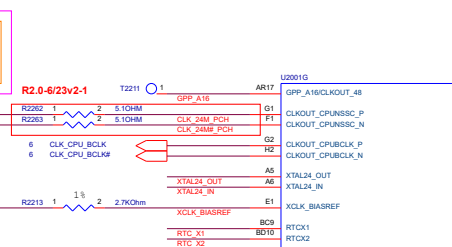
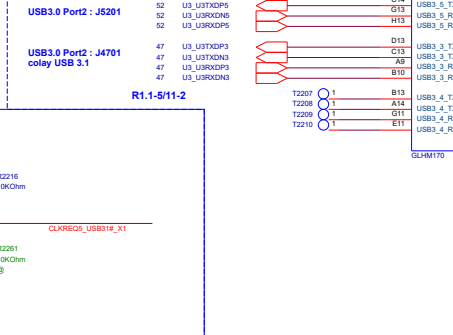
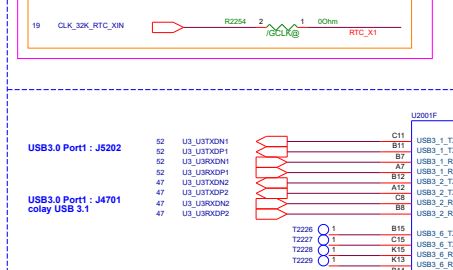
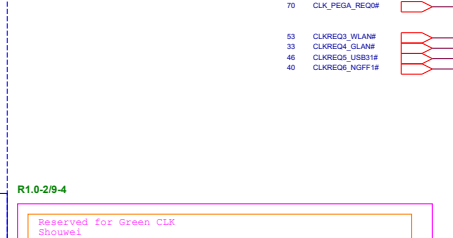
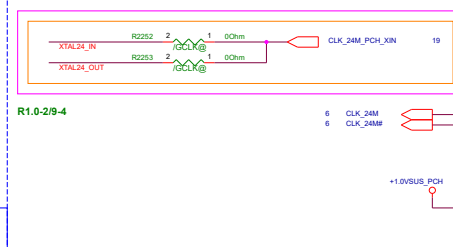
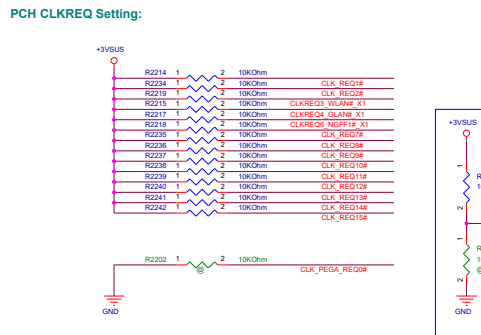
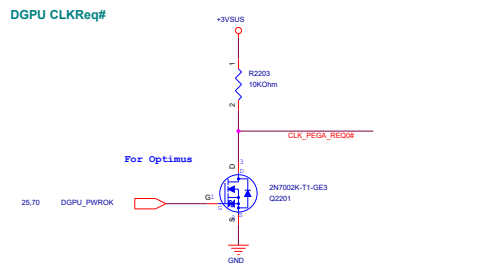
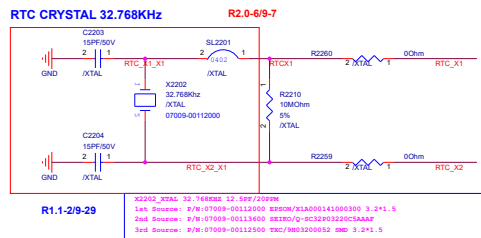
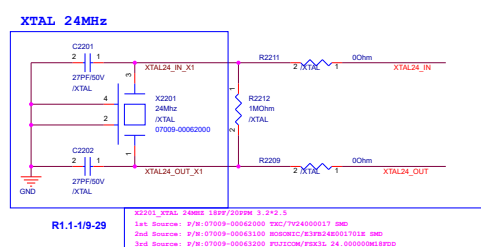


USB Setting

GL552VXK USB Function define
Kabylake HM175

USB 2.0	Function	USB 3.0	Function
USB2_01	USB3.0 IO	USB3_01	USB3.0 IO
USB2_02	USB3.0 IO colay USB3.1	USB3_02	USB3.0 IO colay USB3.1
USB2_03		USB3_03	USB3.0 IO colay USB3.1
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 IO	USB3_05	USB3.0 IO
USB2_06	USB2.0 IO	USB3_06	
USB2_07		USB3_07	
USB2_08		USB3_08	
USB2_09	BT/WLAN		
USB2_10			
USB2_11			
USB2_12			

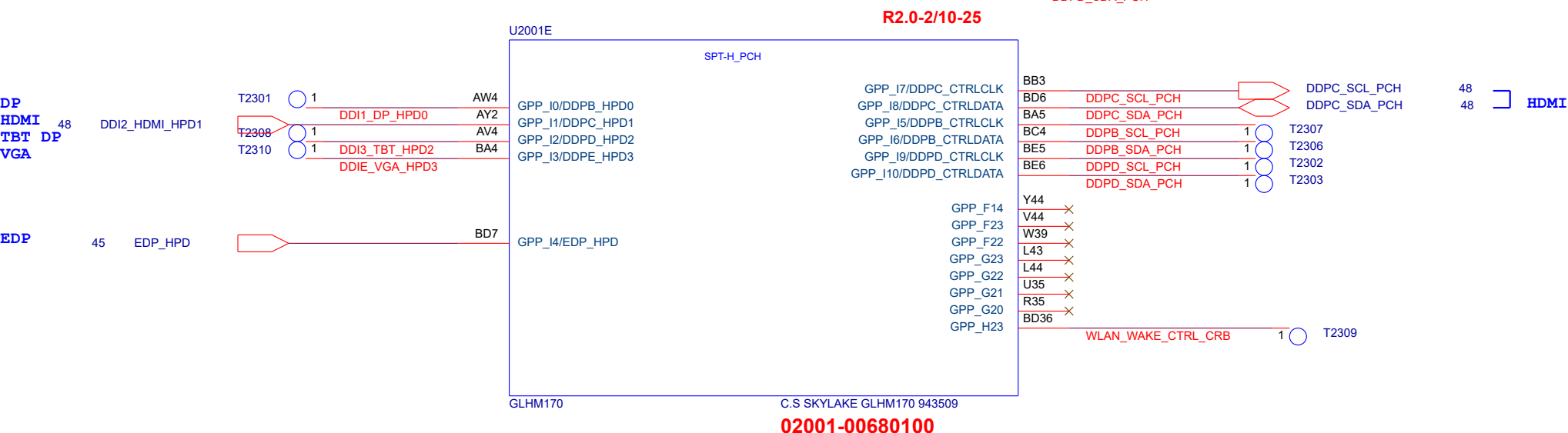
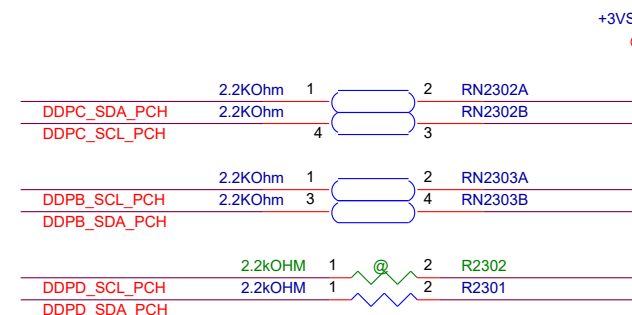




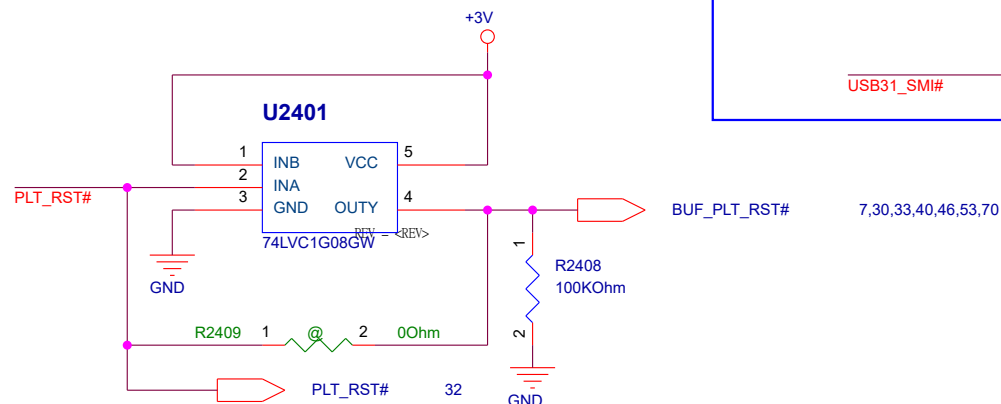
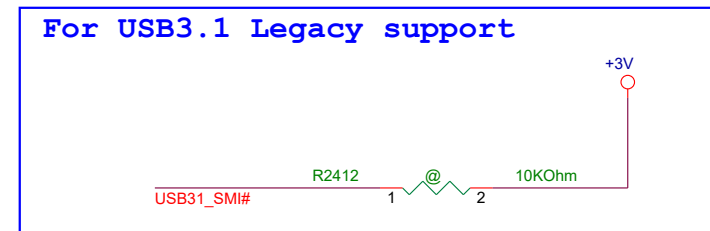
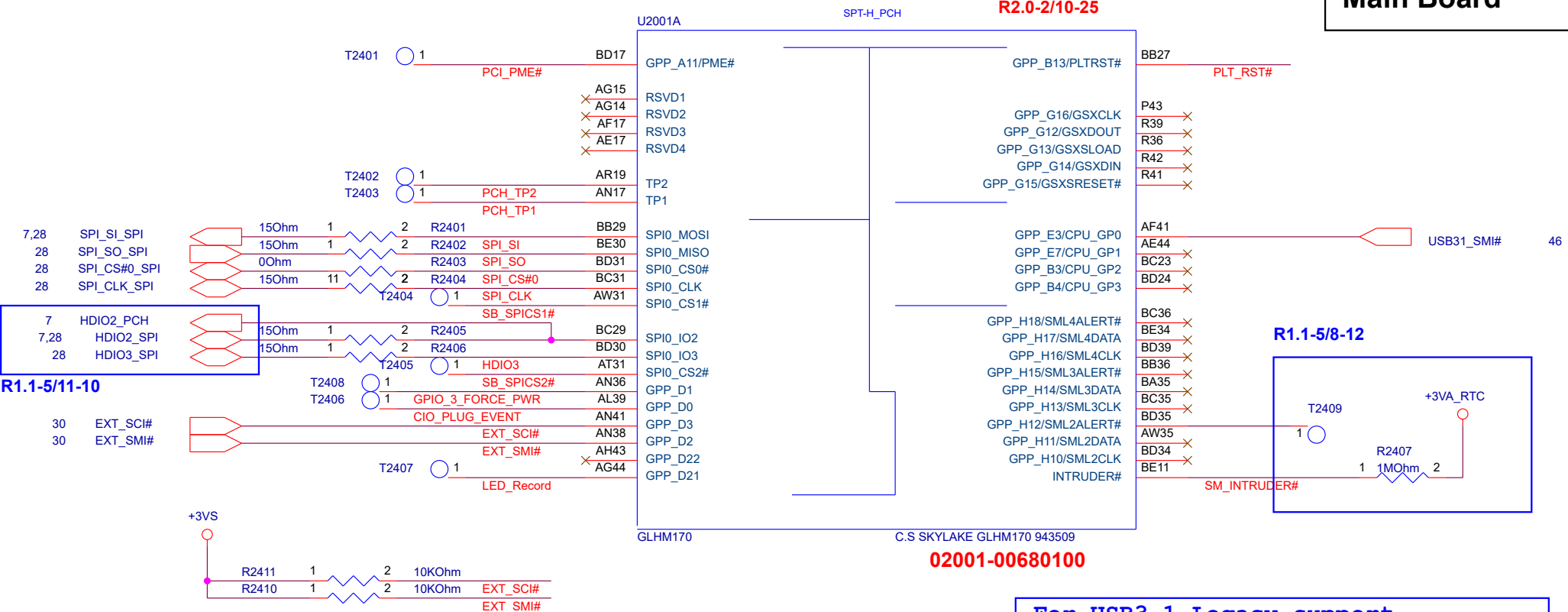
teknisi-indonesia

```
HPD0 to DP
HPD1 to HDMI
HPD2 to TBT DP
HPD3 to VGA
HPD4 to EDP Panel
```

```
DDPD Strap Setting Update :
0 = Port D is not detected (Default)
1 = Port D is detected
20150309
```

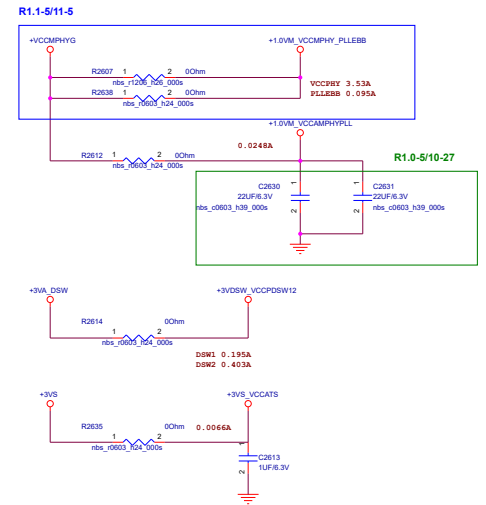
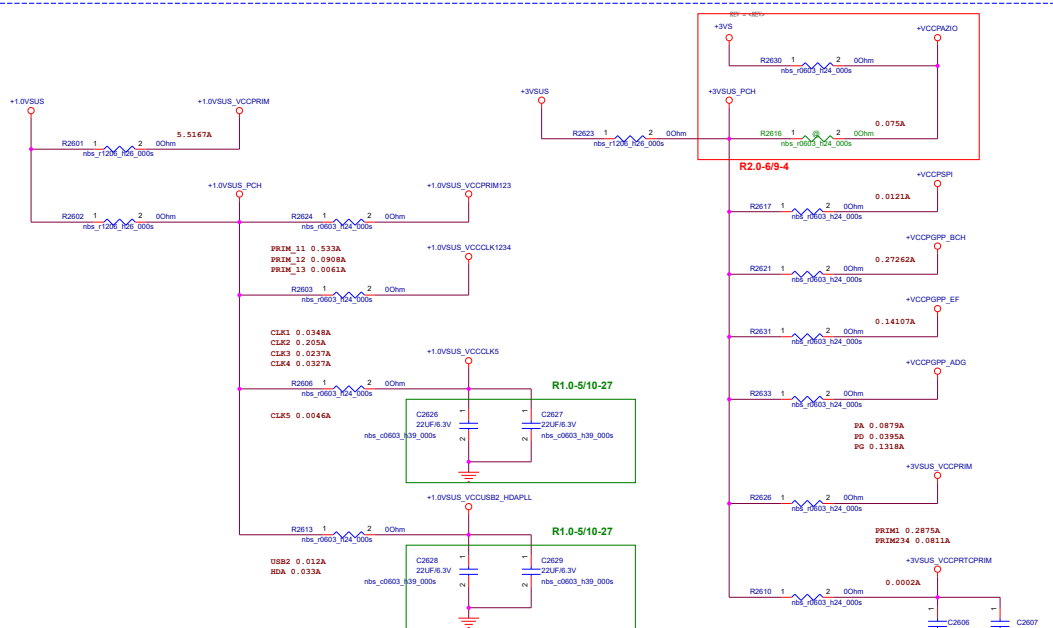
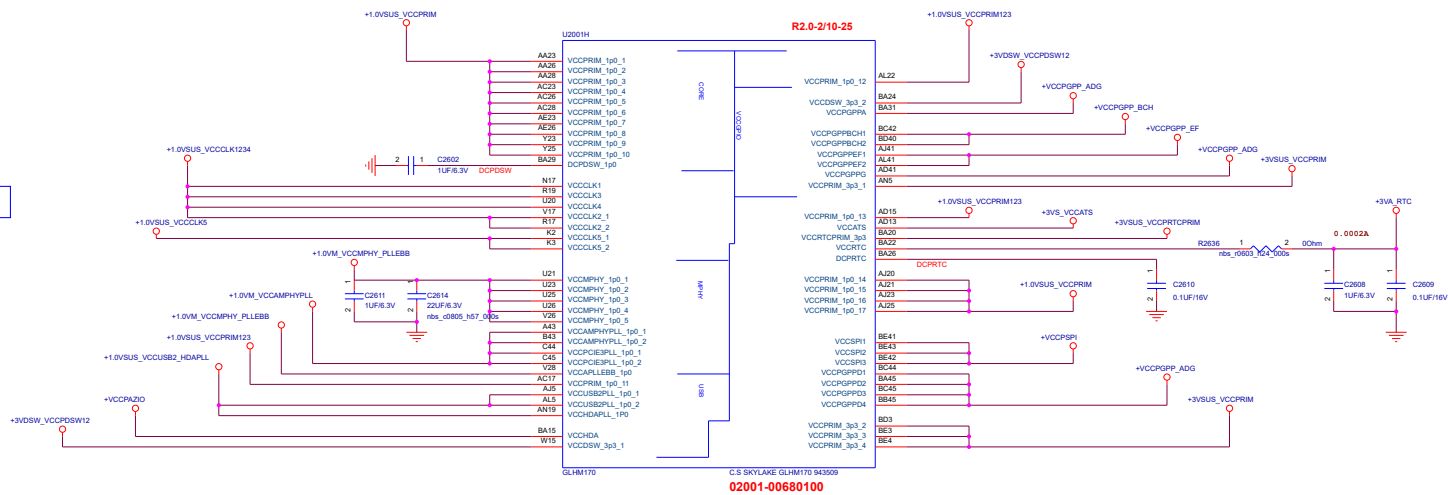


Main Board

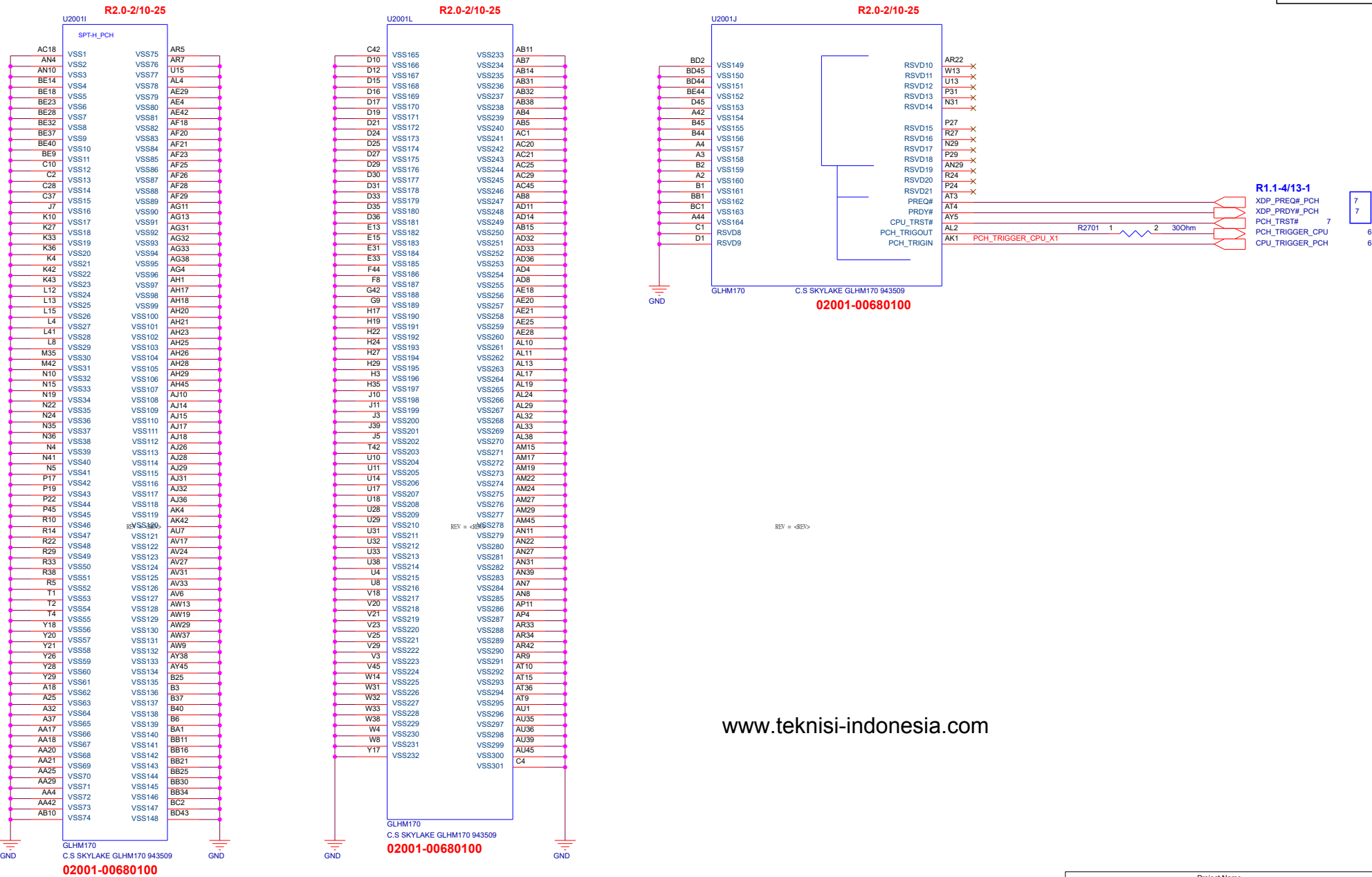




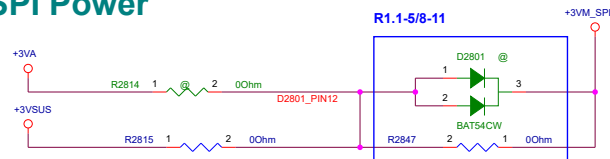
[Modify ALL](#)



Supply	Value	Quantity	Type	Notes	Placement
VccMPHYPLL & VccPCIE3PLL (Pin A43, B43, C44, C45) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	Recommended to be placed <3 mm from edge of package
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccUSB2PLL & VccHDAPLL (Pin A35, A5, AN19) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	
VccCLK5 (Pin K2, K3) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%	
	22 uF	2	Filter Capacitor (Vss) 0805	20%	



SPI Power

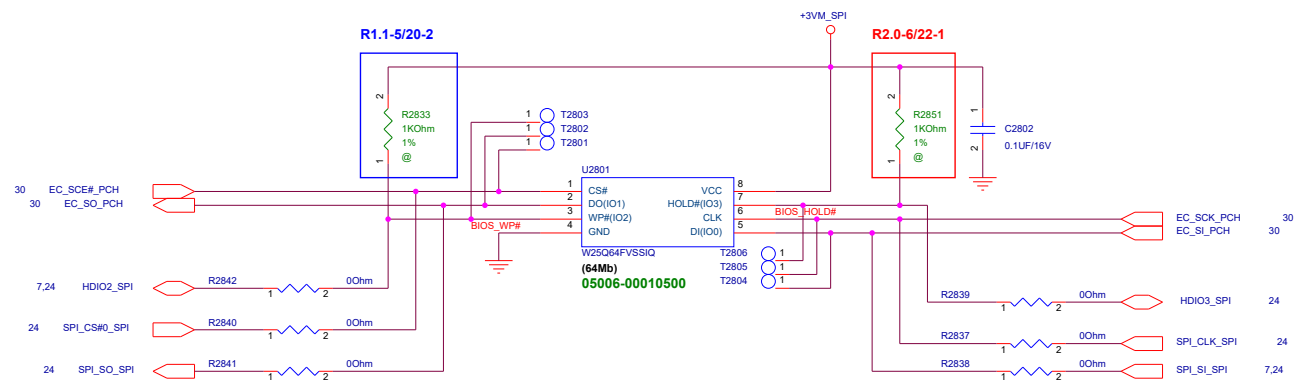


1st SPI ROM

R2.0-3/10-25

U2801_FLASH WINBOND W25Q64FVSSIQ

1st Source: P/N:05006-00010500 FLASH WINBOND W25Q64FVSSIQ

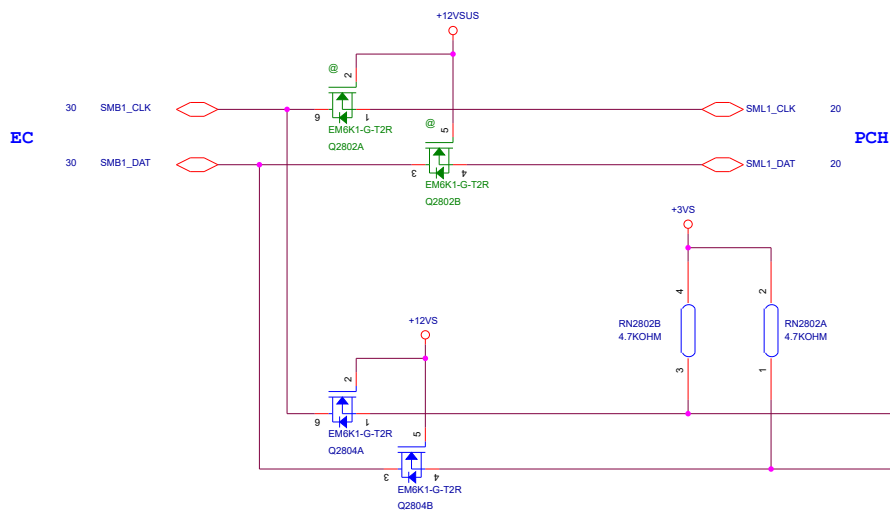


R1.1-5/20-2

R2.0-6/10-2

For ES sample, QS sample need to unmont

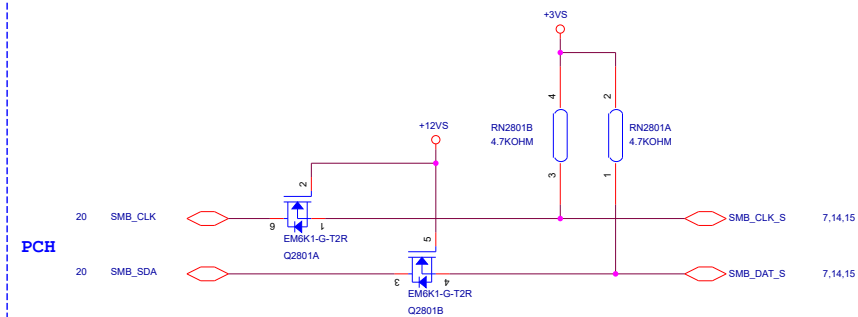
System Management Interface



SMBus Interface

P.14_SO-DIMM CHA-DIMM0 (A0h)

P.15_SO-DIMM CHB-DIMM0 (A4h)



R2.0-6/9-3

CPU,VGA & Power Thermal Sensor

SMB1_CLK_S 50.75,90


SMB1_DAT_S 50.75,90

P.50_CPU Thermal Sensor (90h)

P.75_DGPU Thermal Sensor (96h)

P.90_Power Protection Sensor (7Eh)

ASUS		Project Name	Rev
GL552VXX			2.0
Title : PCH-SPI ROM,OTH			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Wenchu_Shen
Date: Thursday, November 10, 2016	Sheet	28	of 103

		Project Name GL552VXX		Rev 2.0
Title : PCH-XDP				
Size B	Dept.: ASUSTeK COMPUTER INC.		Engineer:	Wenchi_Shen
Date: Thursday, November 10, 2016			Sheet	29 of 103

Only 3V Torlence

```
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
```

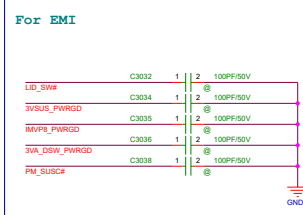
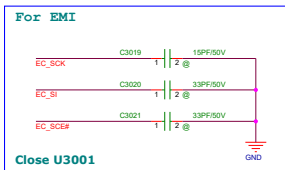
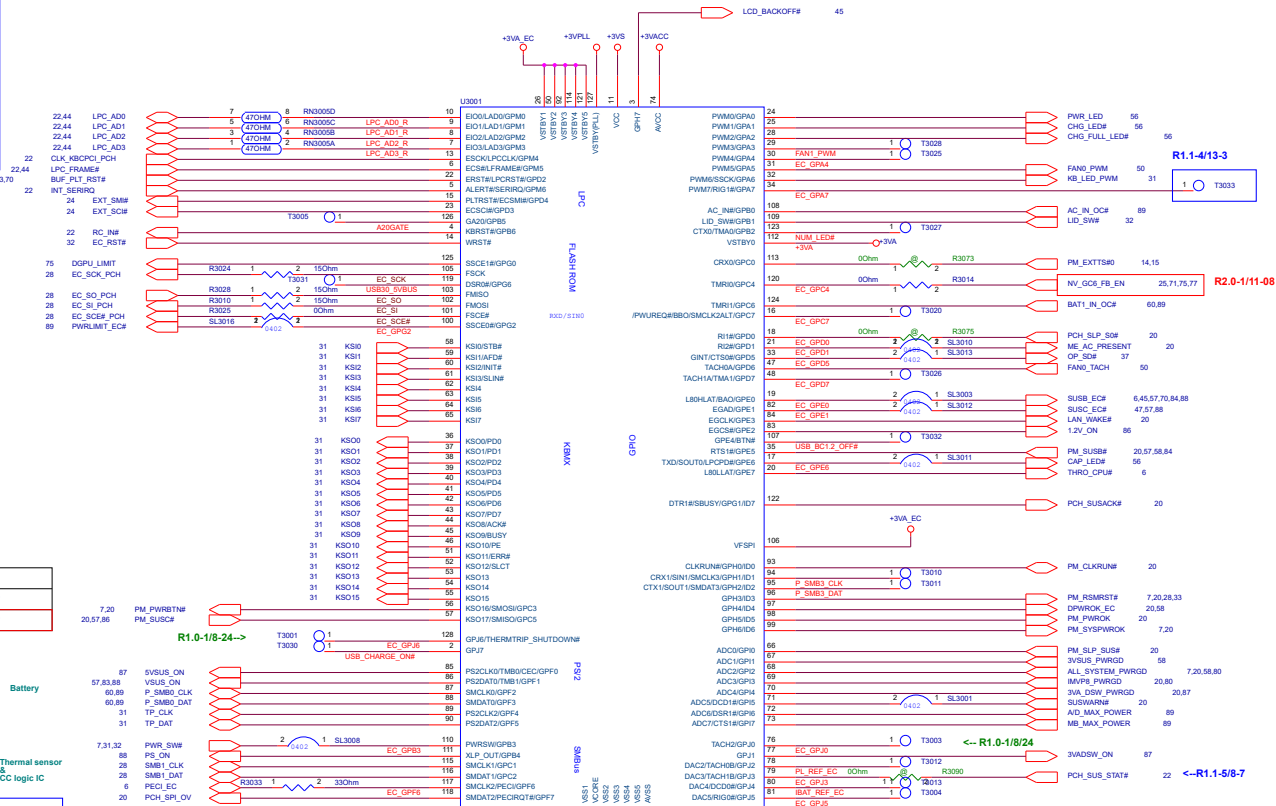
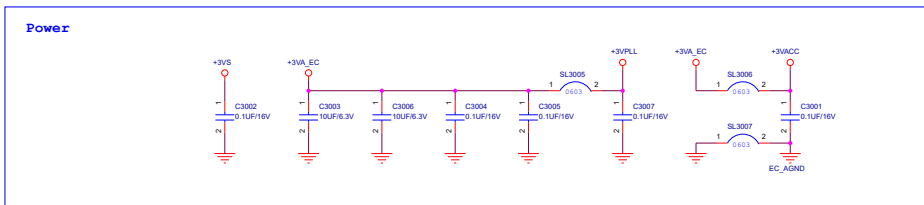
Can be adjusted to
Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

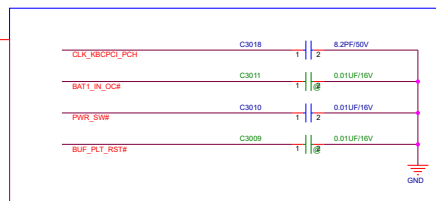
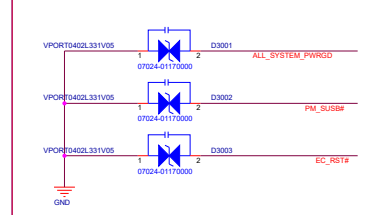
EC Require

ITE Version	ASUS P/N
IT8995E-128/CX	06037-00050500
IT8995E-128/DX	06037-00050700

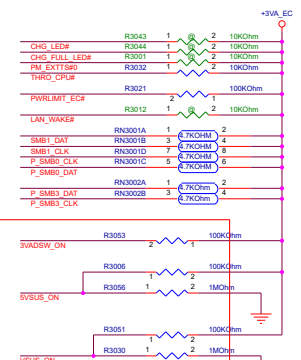
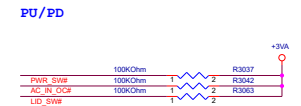
use



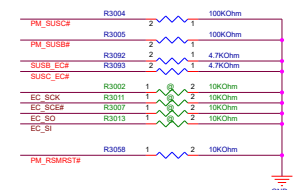
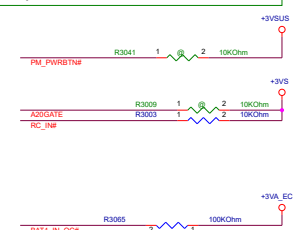
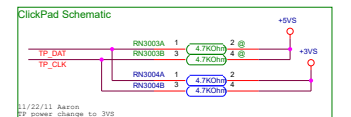
R2.0-6/17-3



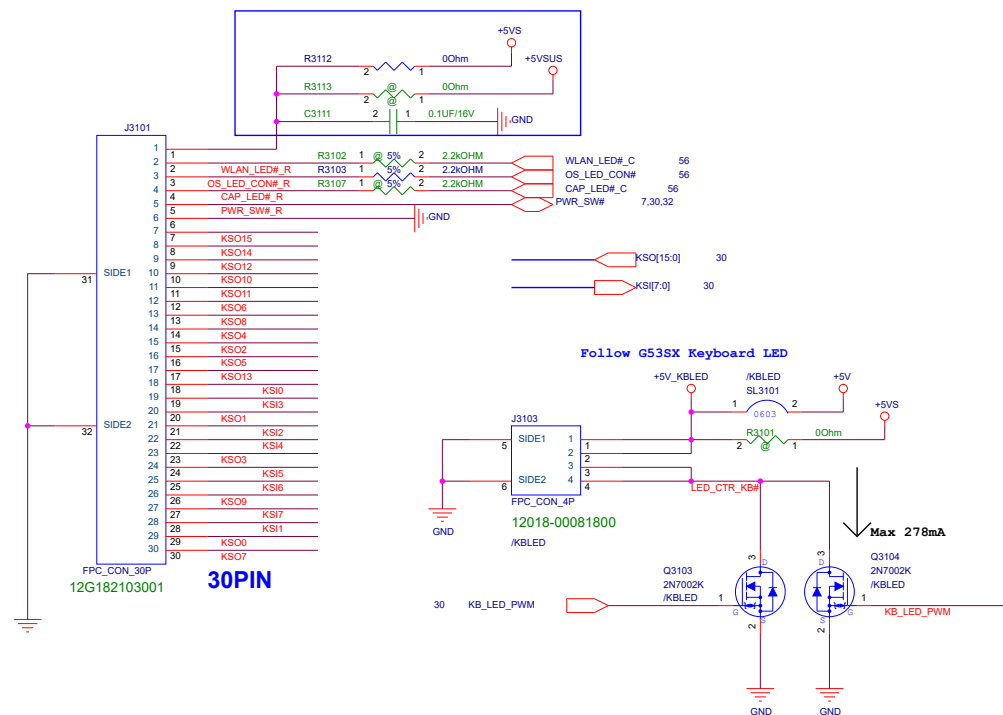
teknisi-indonesia



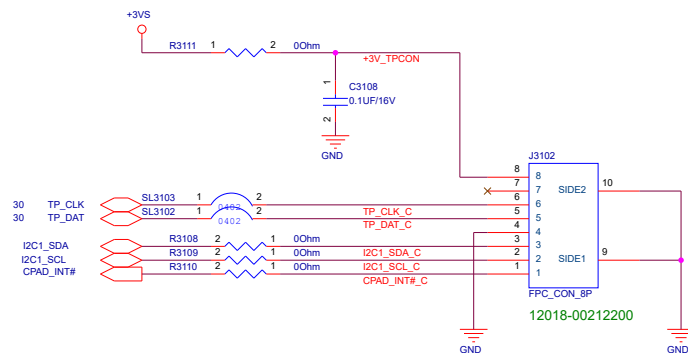
```
for load code
```



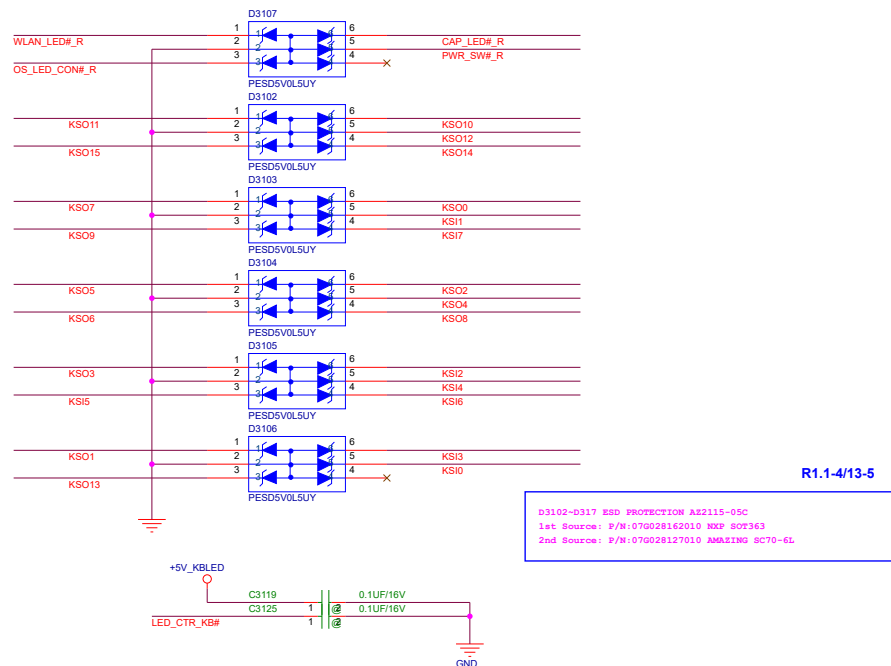
R1.1-5/8-8



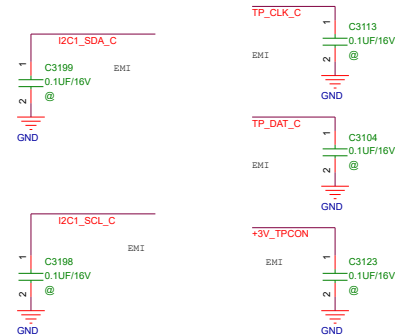
Click touch Pad Connector



For EMI

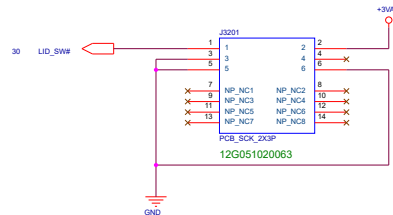
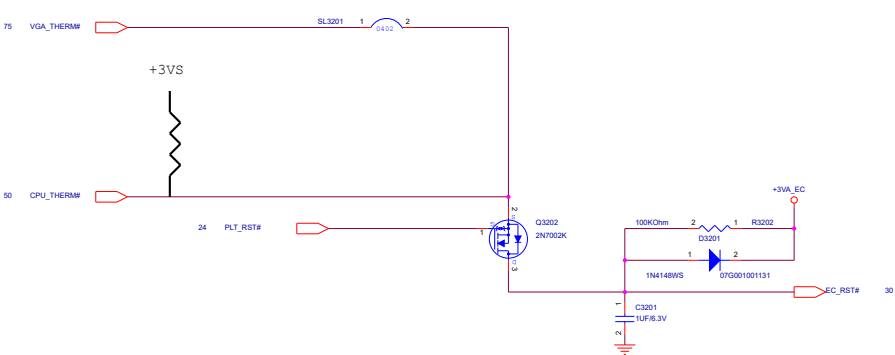


Reserved for EMI

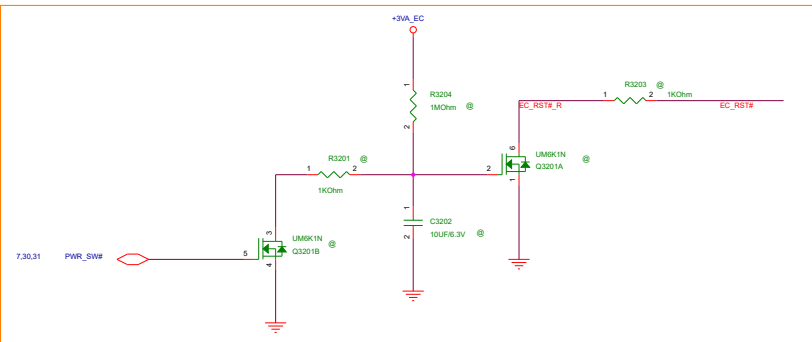


Reset Circuit

Pull up +3VSG through R7507(10kOhm~>100kOhm)
 When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
 The CPU temperature point is protected ahead of time.
 Increasing R7507 value can reduce to affect R5006.

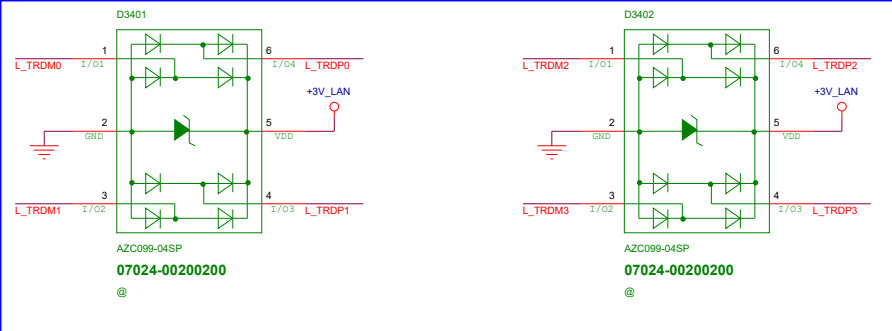


For battery embedded case (press pwr_sw 10sec, then reset ec) (need to modify)



ASUS		Title : RST_Reset Circuit	
ASUSTek COMPUTER INC. NBI		Engineer: Wenchi_Shen	
Size	Project Name	Rev	
B	GL552VXX	2.0	
Date: Thursday, November 10, 2016	Sheet	32	of 100



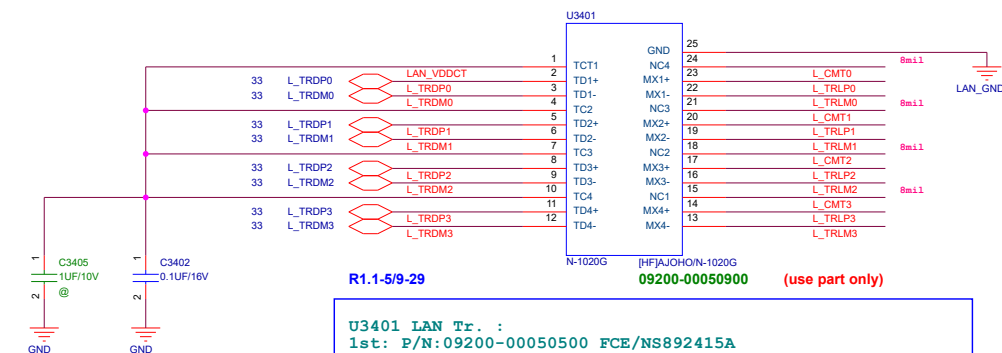


R1.1-4/13-5

D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

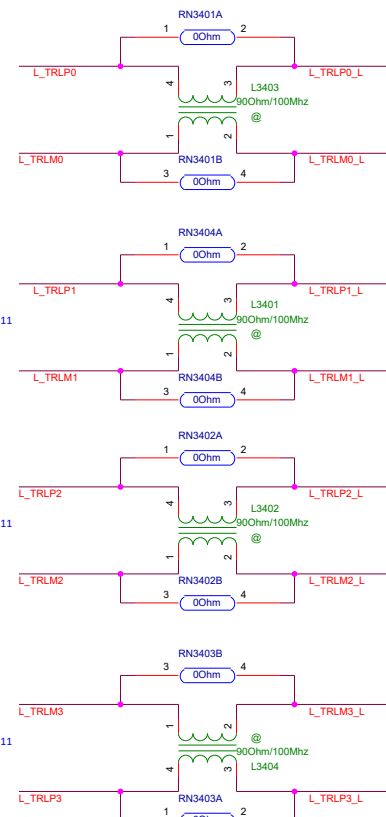
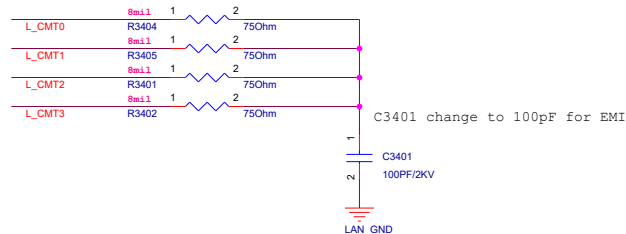


R1.1-5/9-29

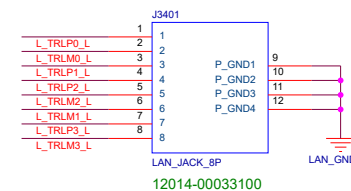
U3401 LAN Tr. :
1st: P/N:09200-00050500 FCE/NS892415A
2nd: P/N:09G051059A20 BOTHHAND/GST5009BMLF

Test Point_LAN Tr.

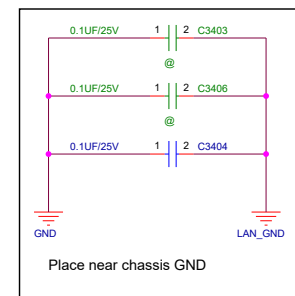
拿掉ATE測試點, 改由layout主動加



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Change GND to LAN_GND FOR EMI





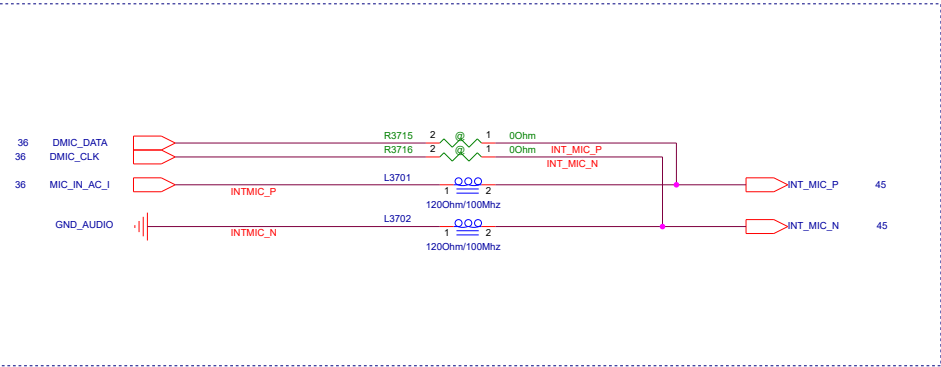
Title : LAN_*****

ASUSTeK COMPUTER INC. NB1

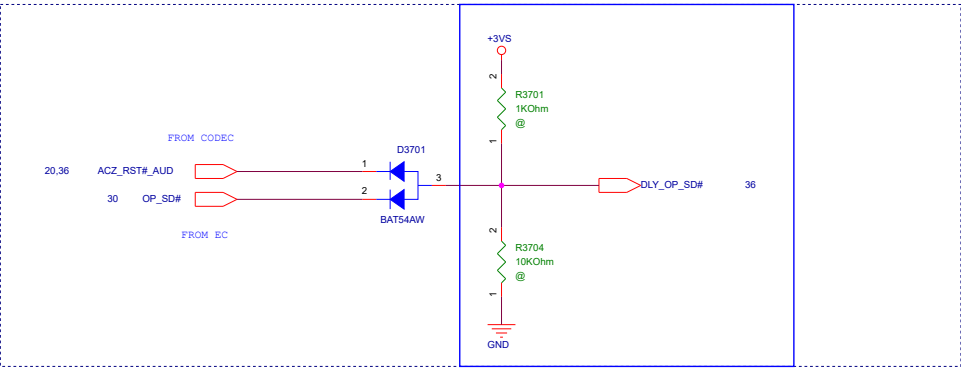
Engineer: Wenchi_Shen

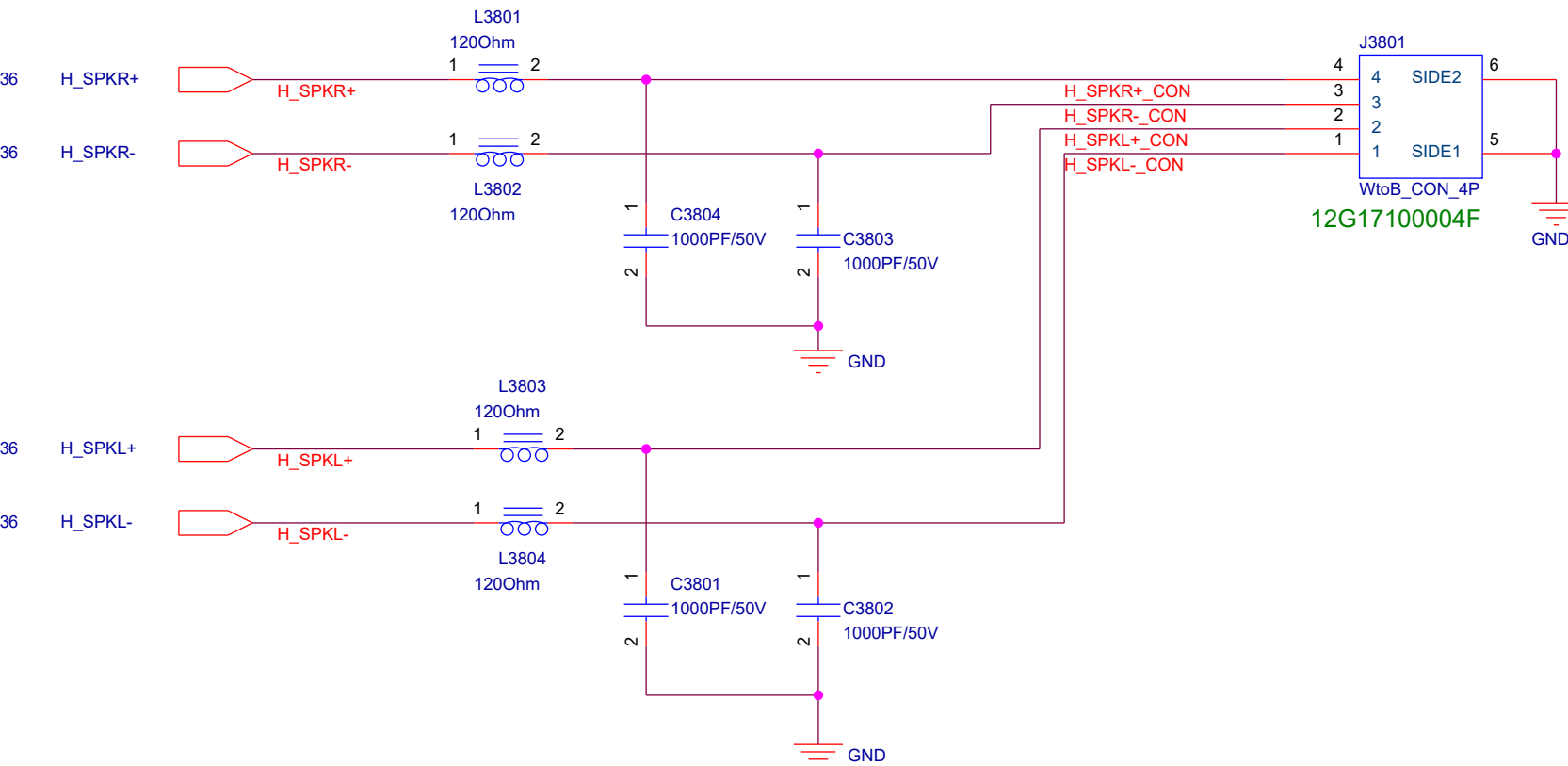
Size	Project Name	Rev
A	GL552VXK	2.0

INTERNAL MICROPHONE




MUTE CONTROL





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		Title : AUD-MIC-IN__R1.4	
ASUSTeK COMPUTER INC. NB1		Engineer: Wenchi_Shen	
Size A	Project Name GL552VXX		Rev 2.0
Date: Thursday, November 10, 2016		Sheet 38	of 103



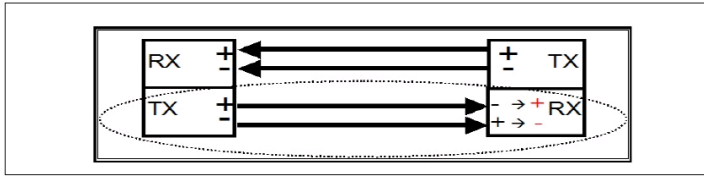
Title : **AUD_WOOFER**

ASUSTeK COMPUTER INC. NB1

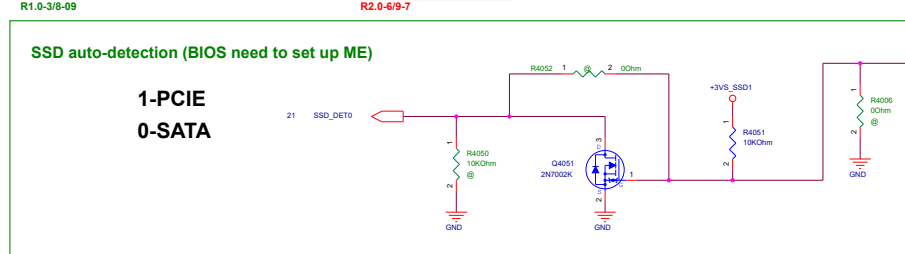
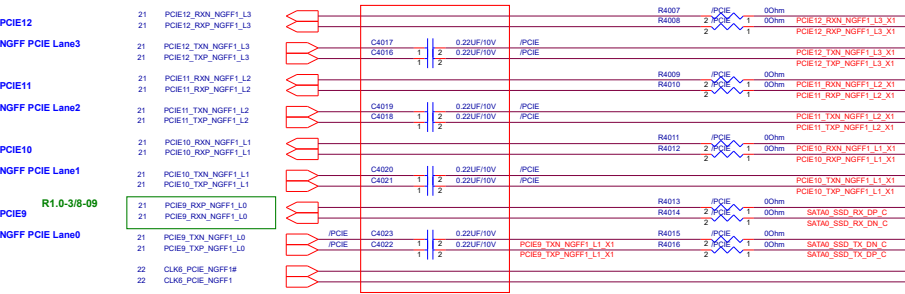
Engineer: **Wenchi_Shen**

Size	Project Name	Rev
A	GL552VXK	2.0

Figure 14-6. Polarity Inversion on a TX to RX Interconnect



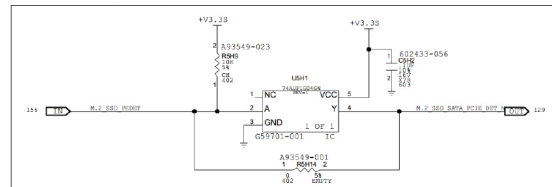
PCIE Device Support Lane Polarity Inversion on RX path
SATA Device Didn't Support Lane Polarity Inversion on RX path



35.3.2.3 PEDET Guidelines

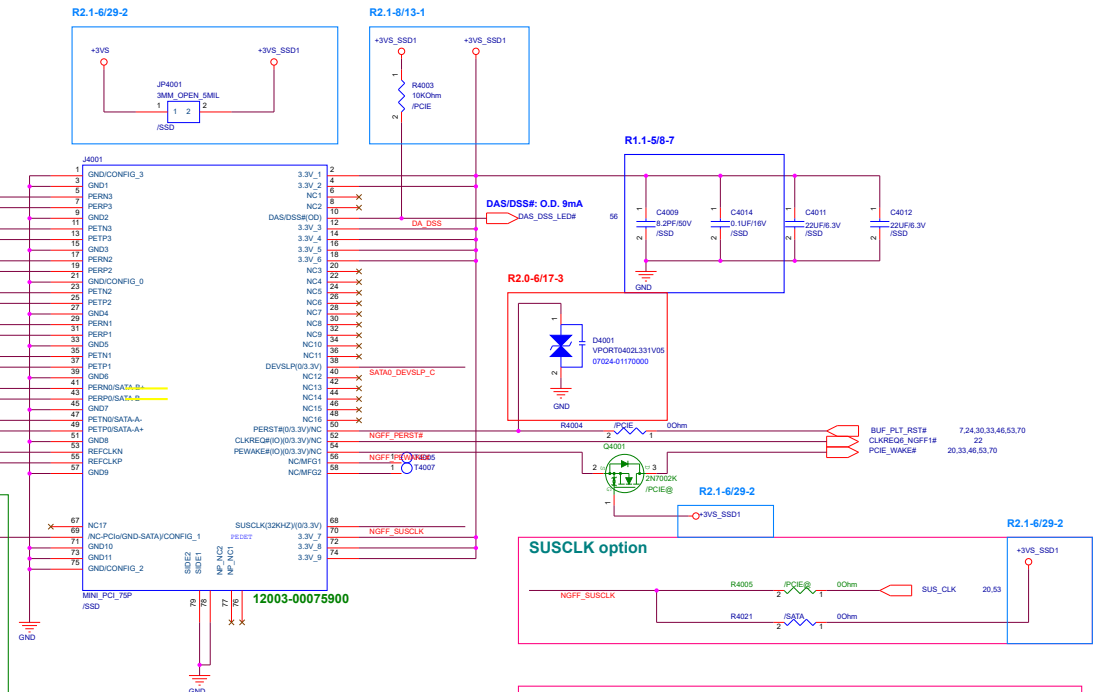
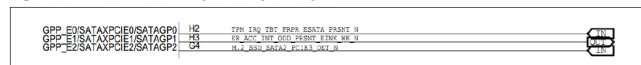
PEDET is the interface detect used by PCH to determine the communication protocol that the M.2 card uses: PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

Figure 35-6. PEDET Circuitry Example



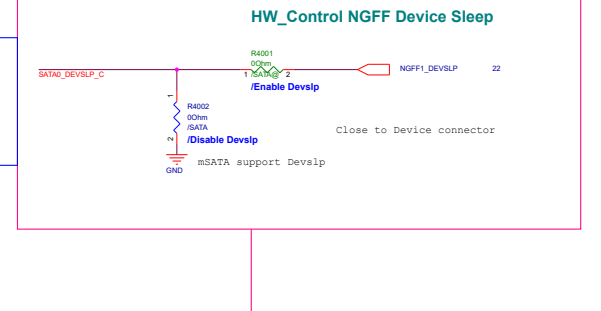
For Kaby Lake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.

Figure 35-7. PEDET Circuitry Polarity Example



R1.1-6/9-29

- J4001_NGFF M-KEY PCIe4 Connector H=3.0mm
- 1st Source: P/N:12003-00075900 ARGOSY/NASMO-S6701-TPH4
- 2nd Source: P/N:12003-00076700 SINGATRON/2NF3001-012111F
- 3rd Source: P/N:12003-00076200 LOTES/APCI0079-P002A
- 4th Source: P/N:12003-00077200 DRAGONSTATE/213MAAA32FA



HW Disable SSD Devslp	Mount R4002=0ohm, Unmount R4001=0ohm
HW Enable SSD Devslp	Unmount R4002=0ohm, Mount R4001=0ohm



Title : CLK_GEN

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size

Project Name

Rev

A

GL552VXK

2.0

Date: Thursday, November 10, 2016

Sheet 41 of 103



Title : CB_RTS5139

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0



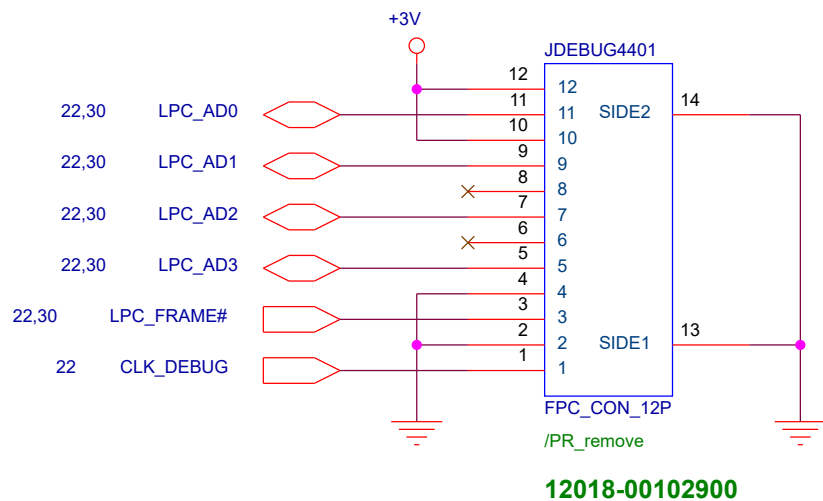
Title : CB_*****

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0

LPC Debug Port



R1.1-4/13-5

JDEBUG4401 Connector (NPI USE)

1st Source: P/N:12018-00102900 ENTERY/6705K-Y12N-20L

2nd Source: P/N:12018-00103000 ACES/51578-01201-002


R1.1-4/13-5

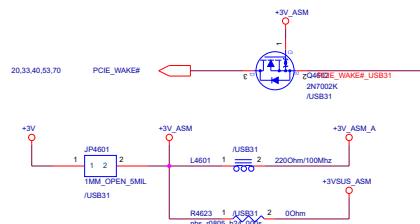
JDEBUG4401 Connector (MP USE)

1st Source: P/N:12018-00102400 P-TWO/196479-12041-3

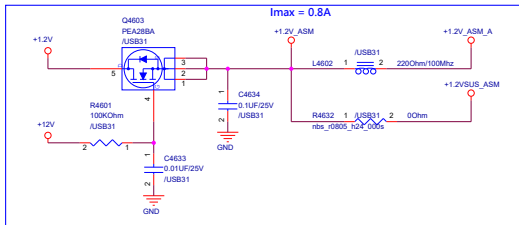
2nd Source: P/N:12018-00102100 ENTERY/6705K-Y12N-00L

3rd Source: P/N:12018-00102300 ACES/51578-01201-001

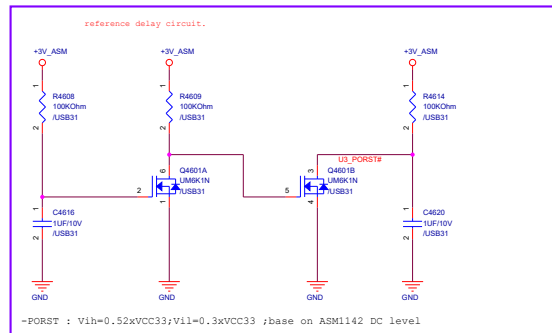
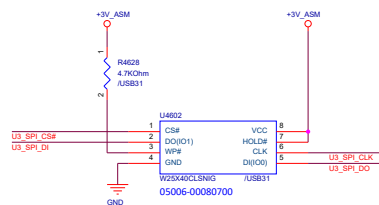
		Title : DEBUG_LPC	
ASUSTeK COMPUTER INC. NB1		Engineer: Wenchi_Shen	
Size A	Project Name GL552VXK		Rev 2.0
Date: Thursday, November 10, 2016		Sheet 44 of 103	



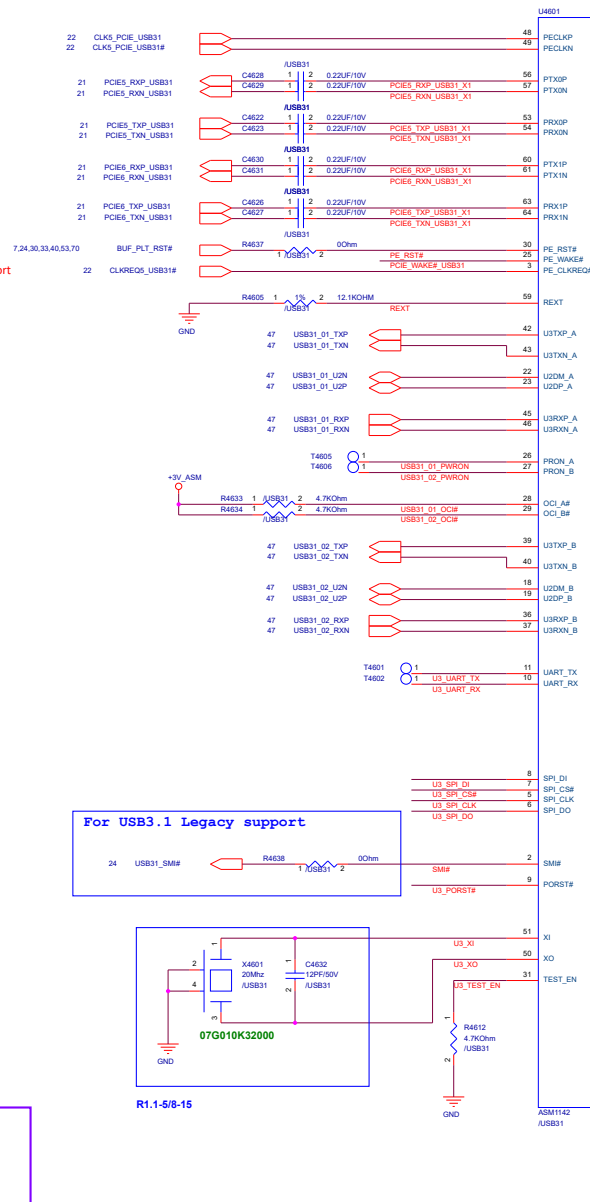
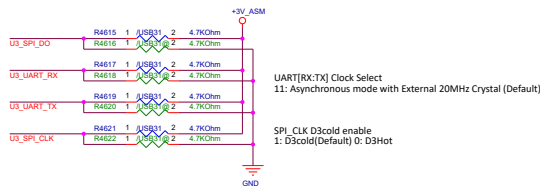
R1.1-5/12-3



CLKREQ 目前ASM1142不support
，在PCH做PD



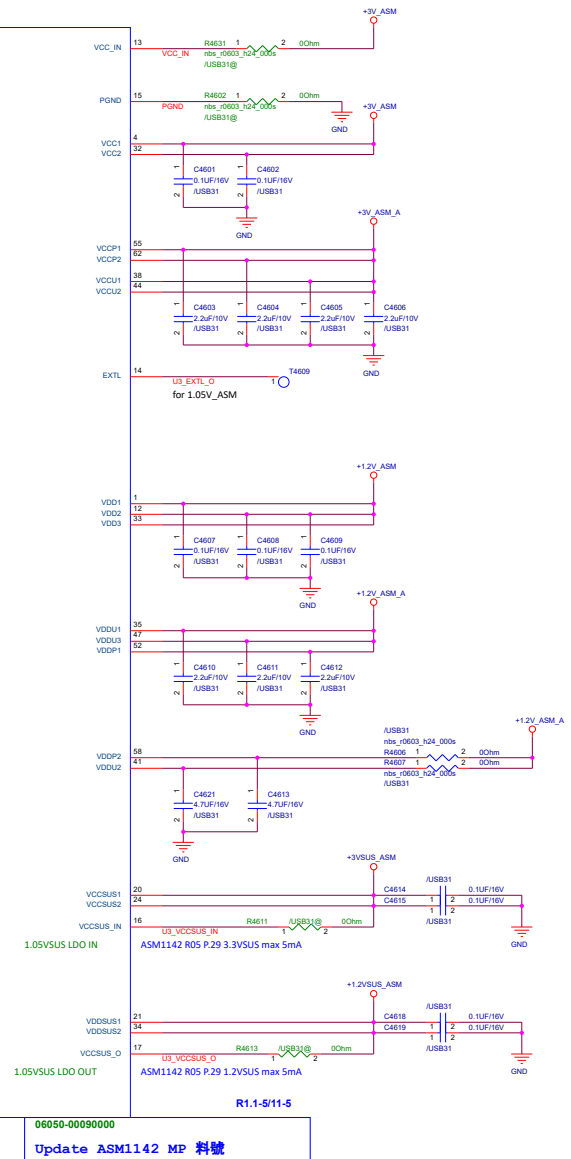
H/W Strapping



R1.1-5/8-15

X4602 ASM 確認用料

07G010K32000	XTAL 20MHz SMD 16PF/10PPM/SIWARD/XTL571100-G47-085	Siward	希華
07G010242000	XTAL 20MHz 3.2*2.5 16PF/10PPM/TXC/TM20000061	TXC	台灣晶技
07009-00080800	XTAL 20MHz SMD 16PF/10PPM SKTECH/FSK3M200000M161	SKC	鑫谷

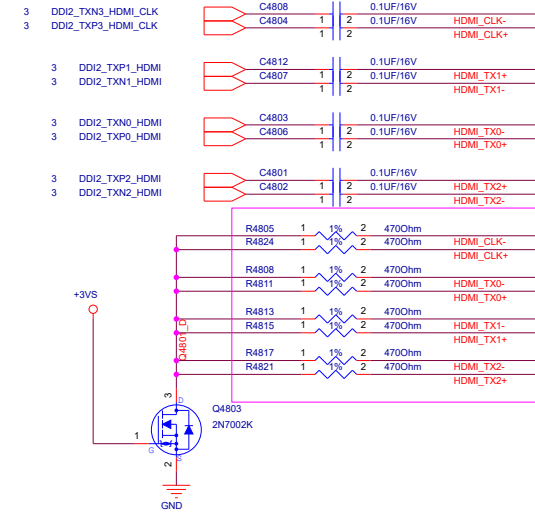


R1.1-5/11-5

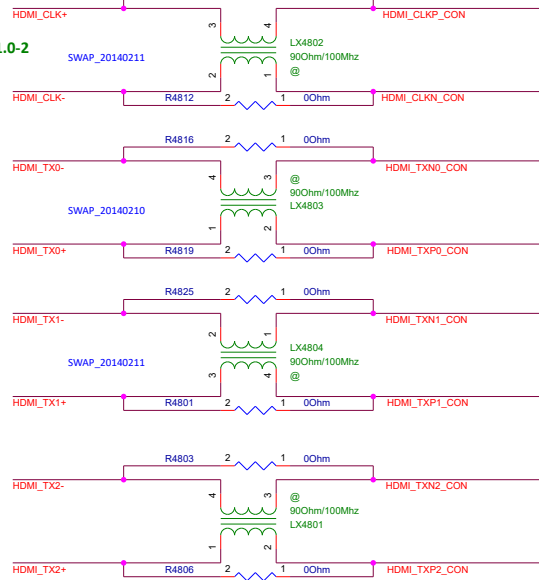
06050-00080000

Update ASM1142 MP 料號

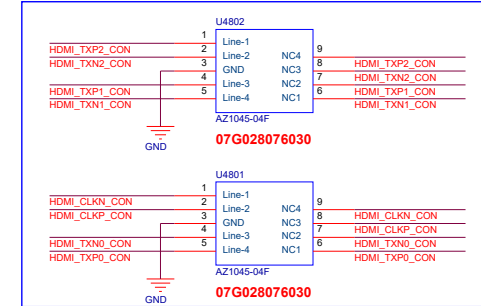
CPU DDIC



R1.0-2



R1.1-17

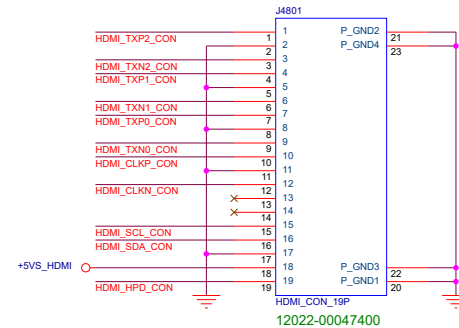
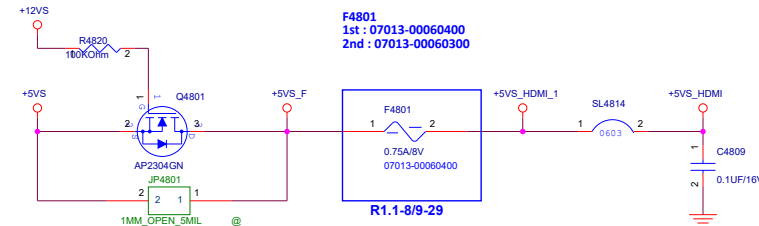
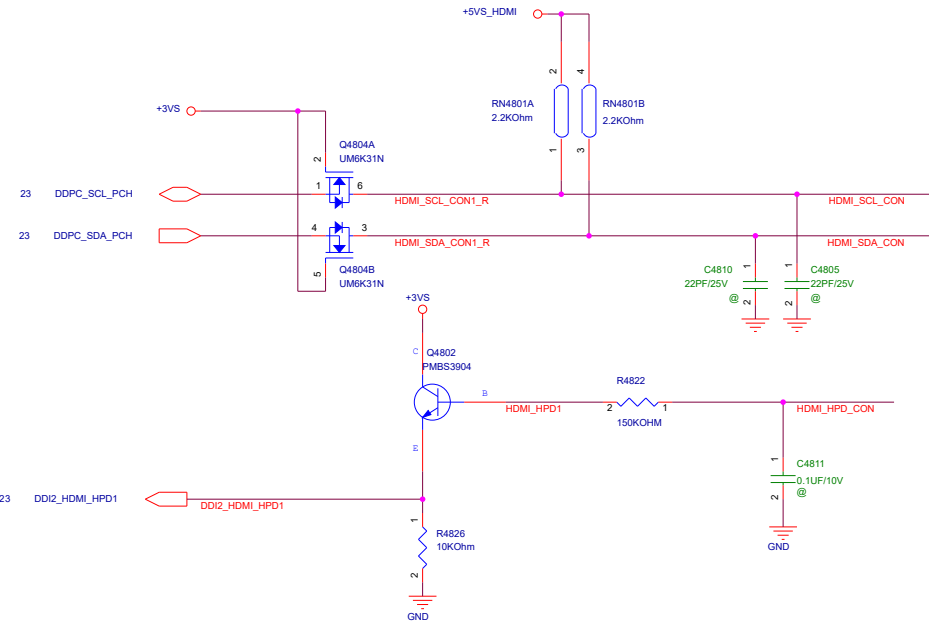


U4801 & U4802 ESD PROTECTION

1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07024-00760000 ESD PROTECTION PUB3BF96

R2.0-6/11-08



12/21/11
For HDMI Design IP R1.4
Del1 Q4801
Add Q4803 07G005047212
F4801=>07G014075310
L4802=>07G013120802



Title : TV_****

ASUSTeK COMPUTER INC. NB1

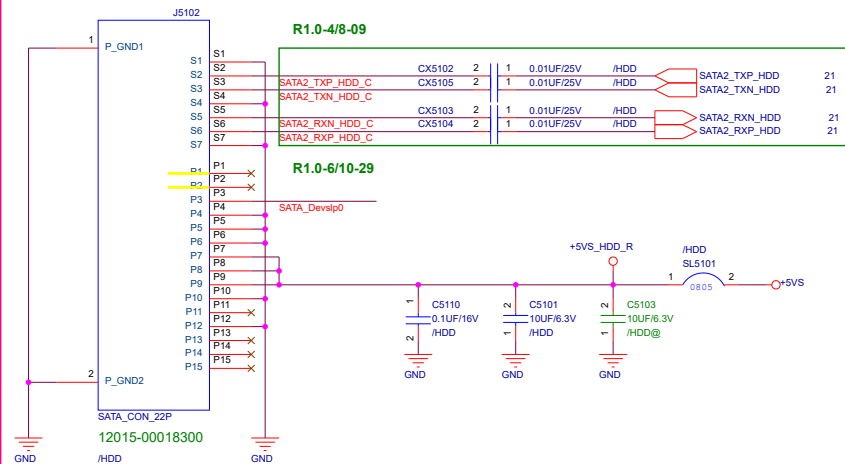
Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0

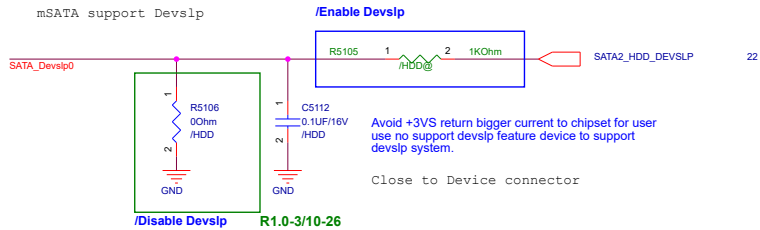
SSD Thermal Sensor Test



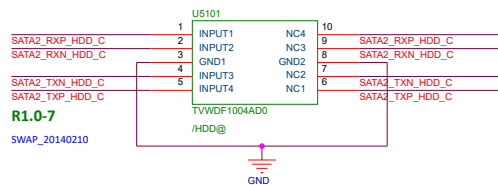
HDD



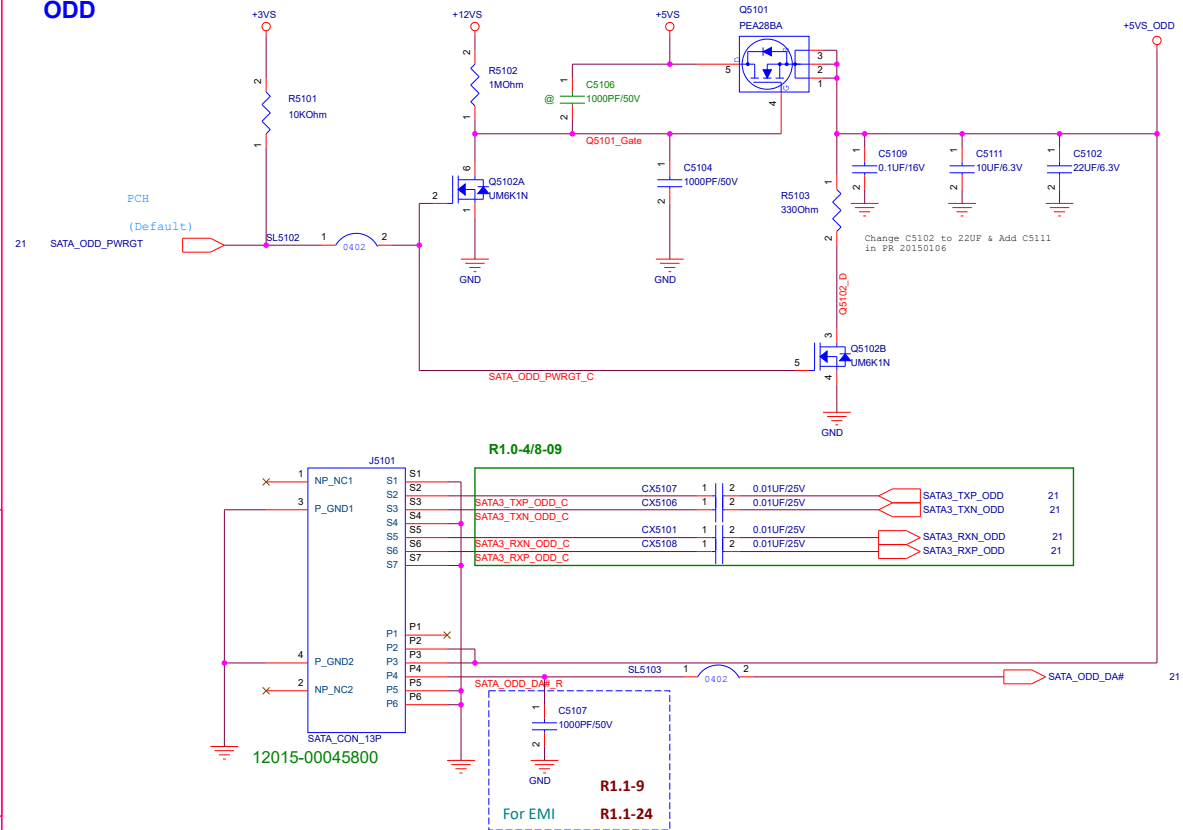
HW_Control SATA Device Sleep



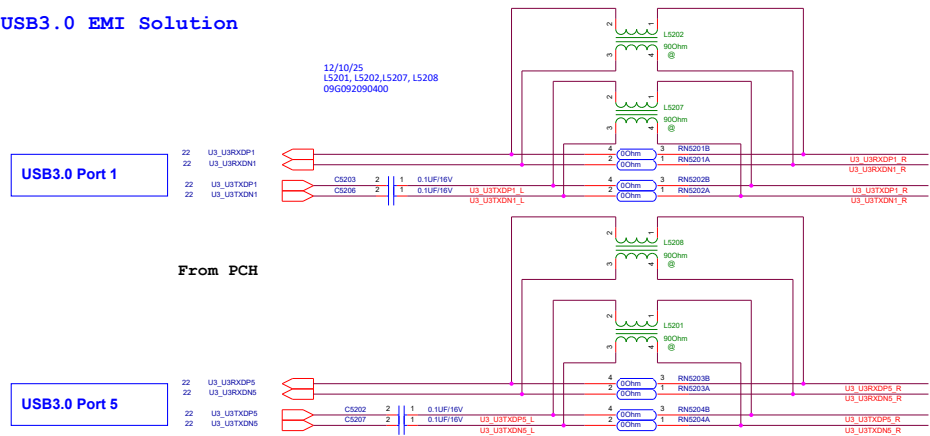
For EMI



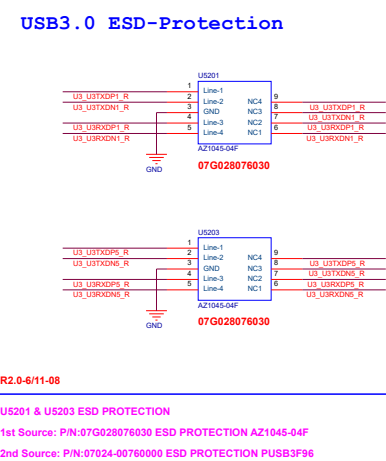
ODD



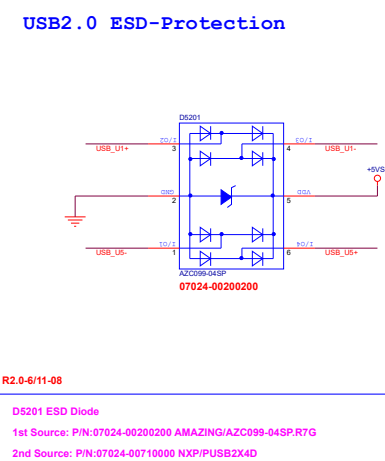
USB3.0 EMI Solution



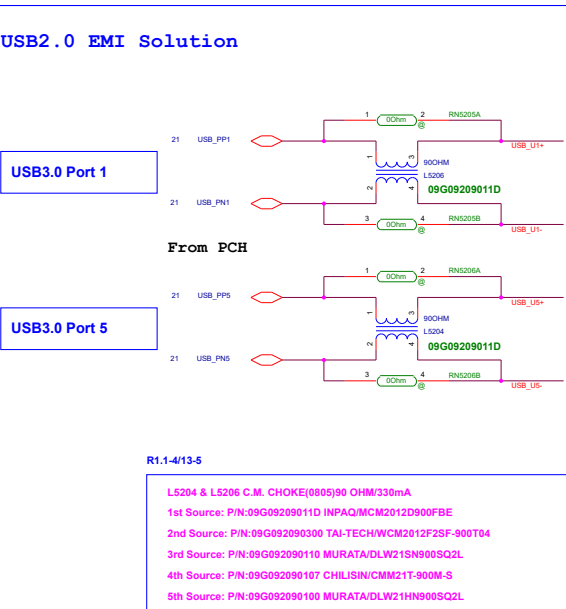
USB3.0 ESD-Protection



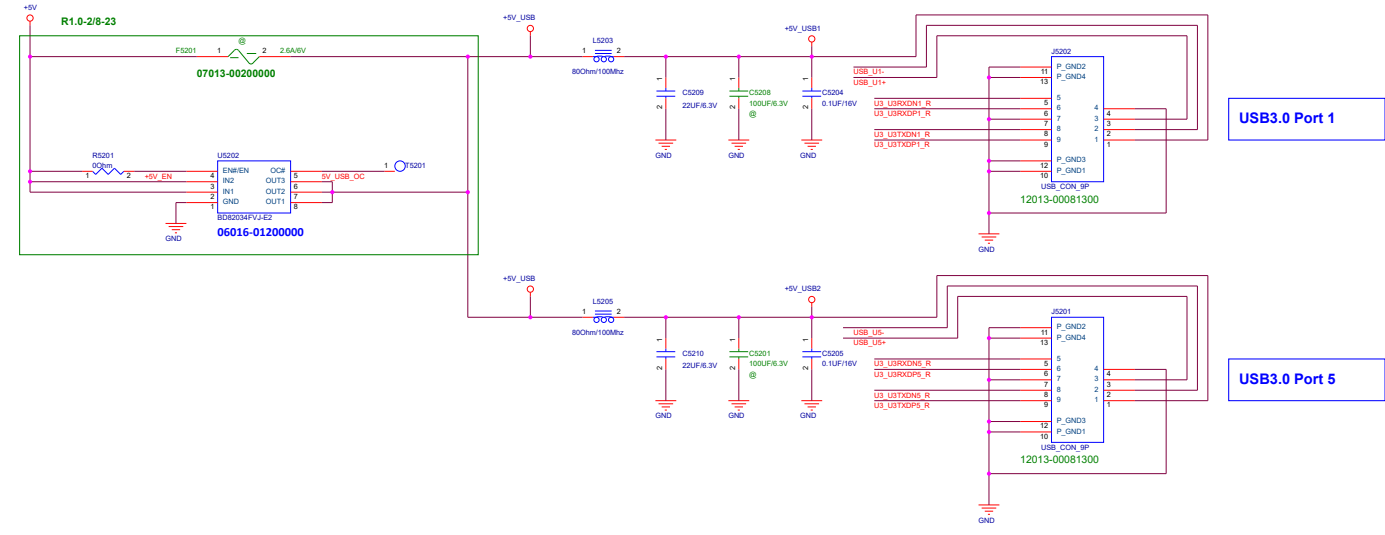
USB2.0 ESD-Protection



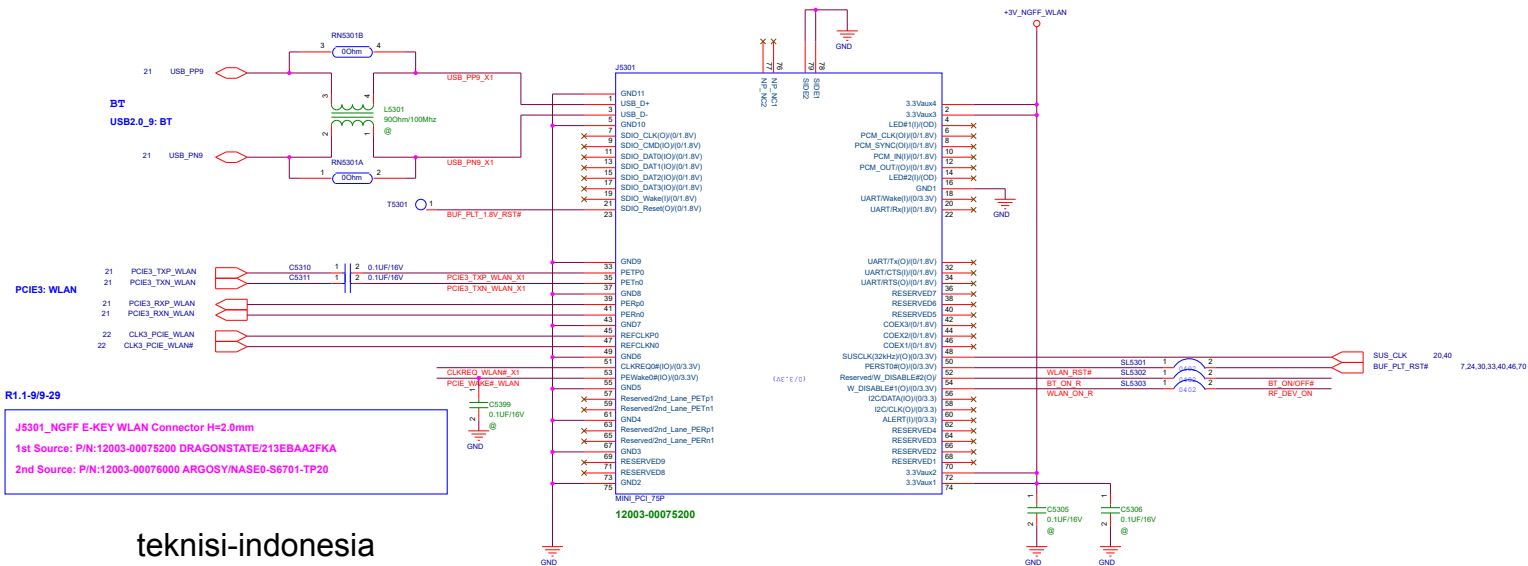
USB2.0 EMI Solution



USB Power Protection & USB3.0 Type-A Connector

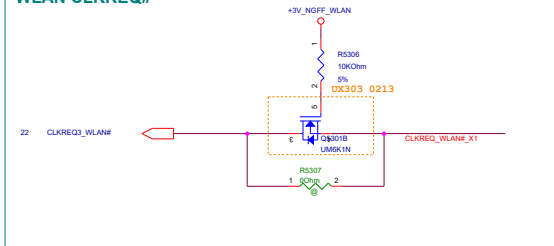


NGFF M.2 TYPE_E-KEY WIFI

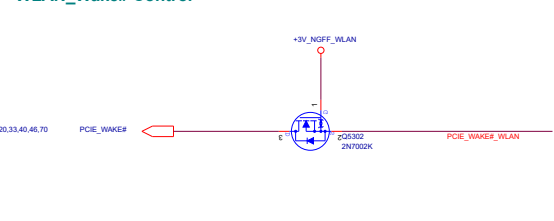


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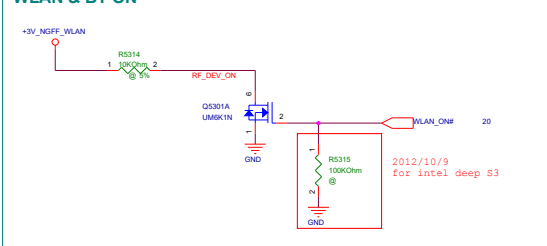
WLAN CLKREQ#



WLAN_Wake# Control



WLAN & BT ON

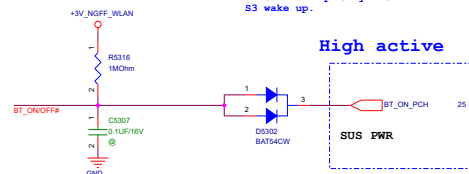


WLAN NUT



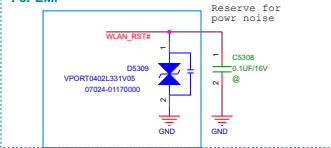
To match WHQL test. Due to BT wake up to spend much time if use +3VS. So, change to +3V, let BT can work quickly when S3 wake up.

High active



Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

For EMI



R2.1-6/26-1

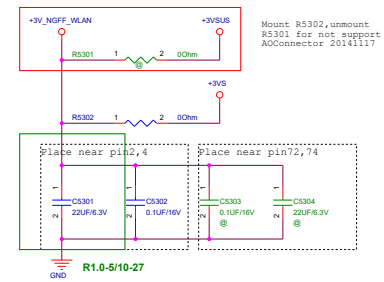
R2.1-6/29-3

D5309_VARISTOR 5V 270PF (0402)
1st Source: P/N:07G0280110 INPAQ
2nd Source: P/N:07019-00070100 INPAQ/MLV5402M04A8/SMD
3rd Source: P/N:07G022005830 THINKING/TVM0G5R5M261R

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

WLAN PWR_ to +3VSUS



74	1.5Vaux	GND	75
72	1.5Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PERn1	67
64	GPIO0 NFC Reset# (MSPIC07)(I/O)(3.3V)	Reserved/2nd Lane PERp1	65
62	NFC I2C IRQ (MSPIC05)(I/O)(3.3V)	GND	63
60	NFC I2C SM CLK (I/O)(3.3V)	Reserved/2nd Lane PERn1	61
58	NFC I2C SM DATA (I/O)(3.3V)	Reserved/2nd Lane PERp1	59
56	W_DISABLE# (I/O)(3.3V)	GND	57
54	Reserved/W_DISABLE# (I/O)(3.3V)	PEWake# (I/O)(3.3V)	55
52	PERST# (I/O)(3.3V)	CLKREQ# (I/O)(3.3V)	53
50	SUSCLK (3.3V) (I/O)(3.3V)	GND	51
48	CODEX1 (7)(0/1.8V)	REFCLKN0	49
46	CODEX2 (7)(0/1.8V)	REFCLKP0	47
44	CODEX3 (7)(0/1.8V)	GND	45
42	CLKH CLK	PERn0	43
40	CLKH DATA	PERp0	41
38	CLKH RESET (I/O)(3.3V)	GND	39
36	UART CTS (I/O)(3.3V)	PERn0	37
34	UART RTS (I/O)(3.3V)	PERp0	35
32	UART TX (I/O)(3.3V)	GND	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART RX (I/O)(3.3V)	SDIO Reset (I/O)(3.3V)	23
20	UART Wake (I/O)(3.3V)	SDIO Wake (I/O)(3.3V)	21
18	GND	SDIO DAT# (I/O)(3.3V)	19
16	LED2 (I/O)(0)	SDIO DATA# (I/O)(3.3V)	17
14	PCM_OUT (I/O)(3.3V)	SDIO DATA (I/O)(3.3V)	15
12	PCM_IN (I/O)(3.3V)	SDIO DATA# (I/O)(3.3V)	13
10	PCM_SYNC (I/O)(3.3V)	SDIO CMD# (I/O)(3.3V)	11
8	PCM_CLK (I/O)(3.3V)	SDIO CMD (I/O)(3.3V)	9
6	LED1 (I/O)(0)	GND	7
4	1.5Vaux	USB_D-	5
2	1.5Vaux	USB_D+	3
		GND	1



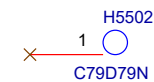
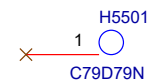
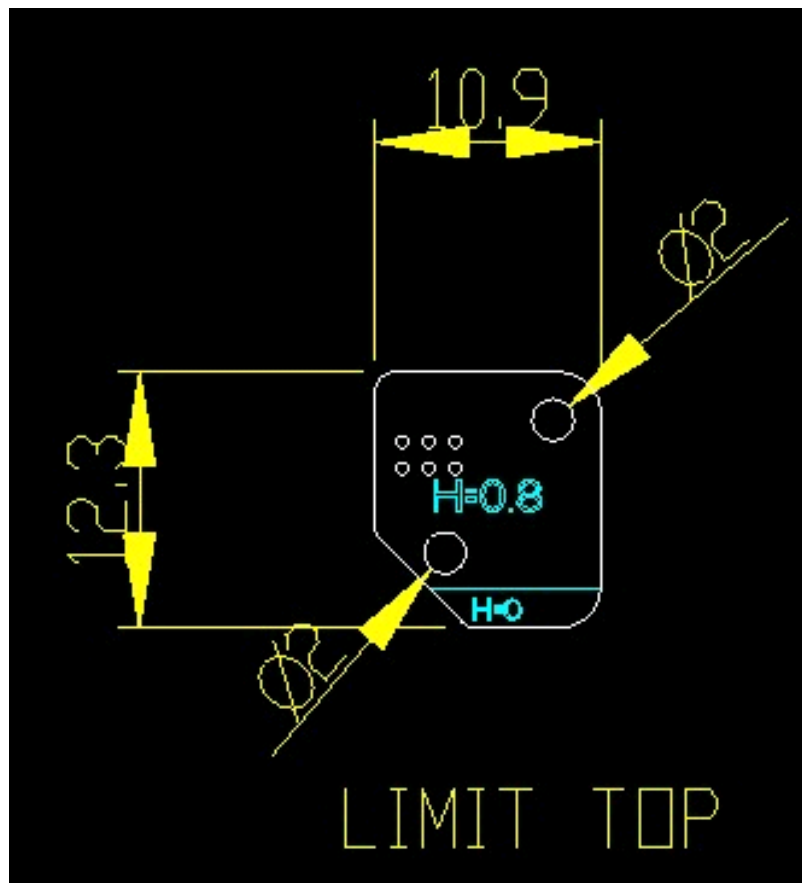
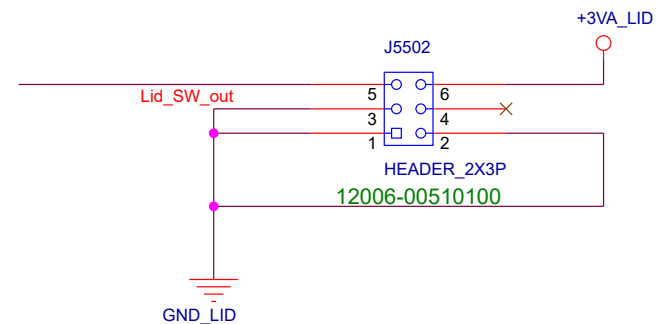
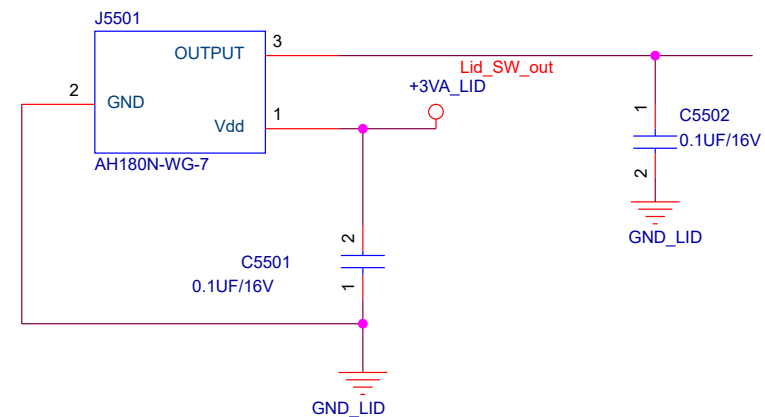
Title : *****

ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

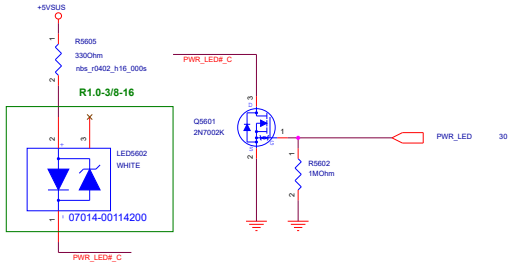
Size	Project Name	Rev
A	GL552VXK	2.0

LID Switch

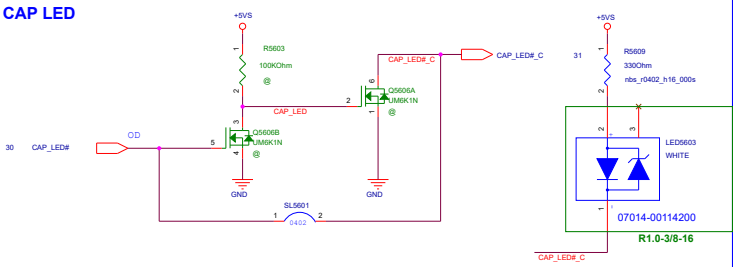


ASUS		Title : Lid_SW_BD	
ASUSTeK COMPUTER INC. NB1		Engineer: Wenchi_Shen	
Size A	Project Name GL552VXX		Rev 2.0
Date: Thursday, November 10, 2016		Sheet 55	of 103

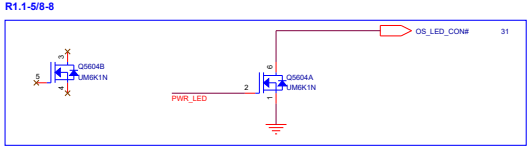
POWER LED



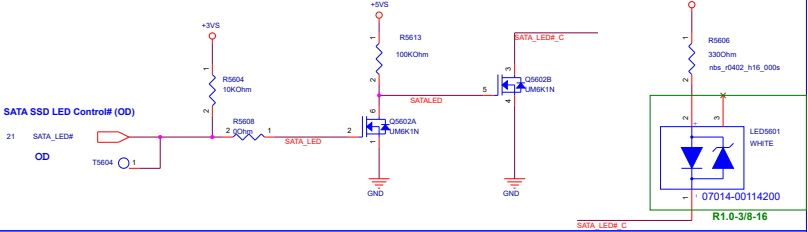
CAP LED



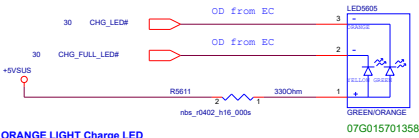
OS_LED#



HDD LED



Charger LED

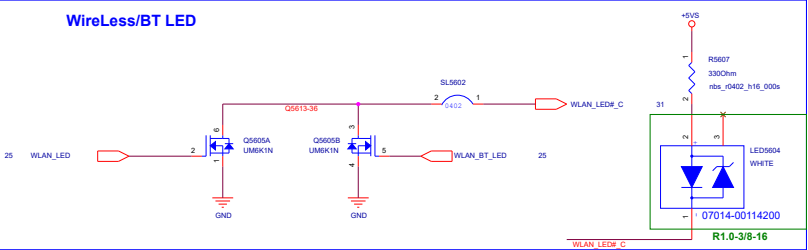


LED5605_ORANGE LIGHT Charge LED

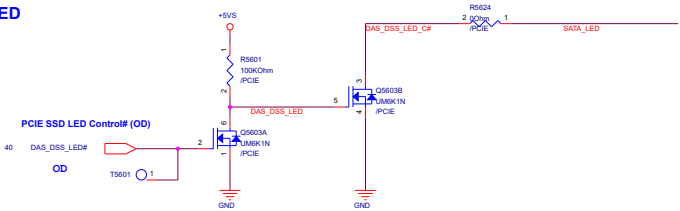
1st Source: P/N:07G015701358 12-22/S2G6C-C30/2C

2nd Source: P/N:07014-00140000 LTST-S326KGKPKT-PE

WireLess/BT LED

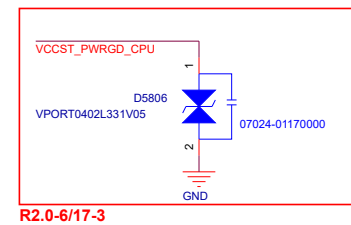
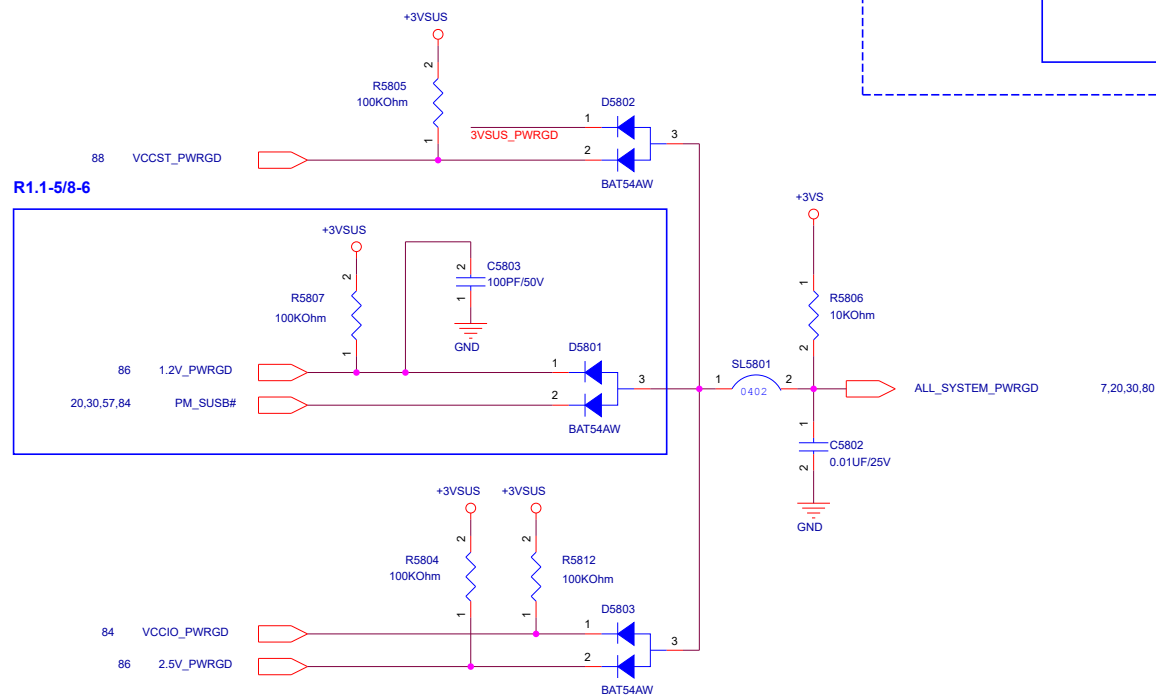
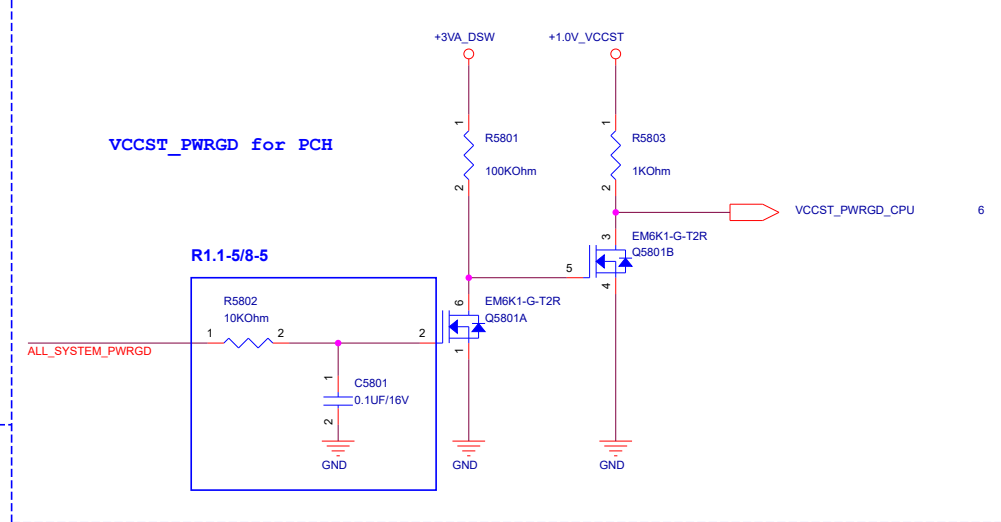
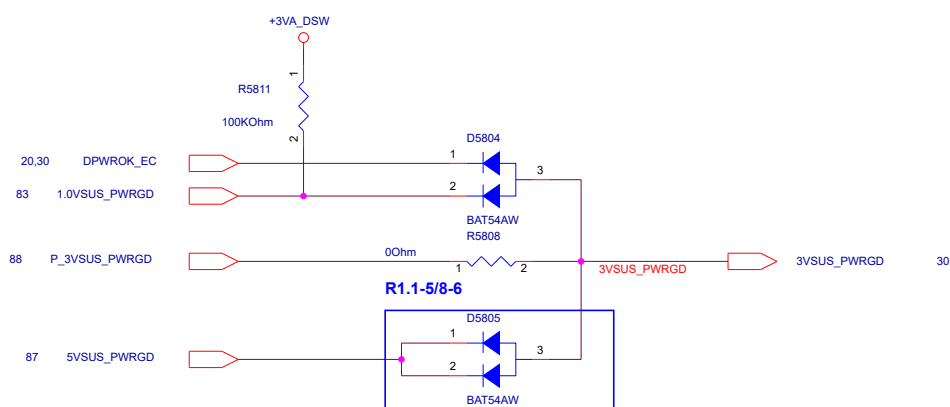


SSD LED



SATALED#	OD O	The default use of this pin is GPIO45. Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. SGPIO Reference Clock: The SATA controller uses rising edges of
----------	------	--





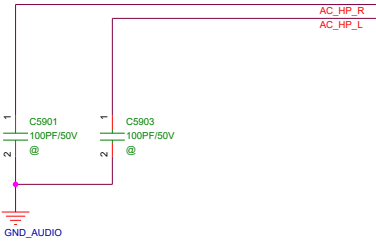
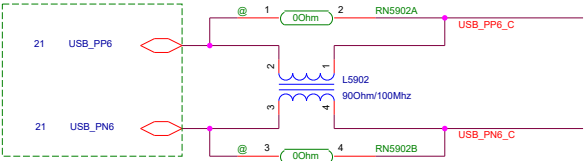
To I/O Board

R1.1-5/11-3

L5902 Choke

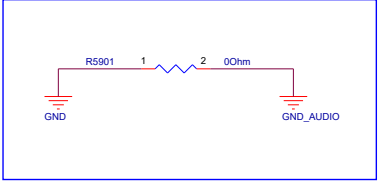
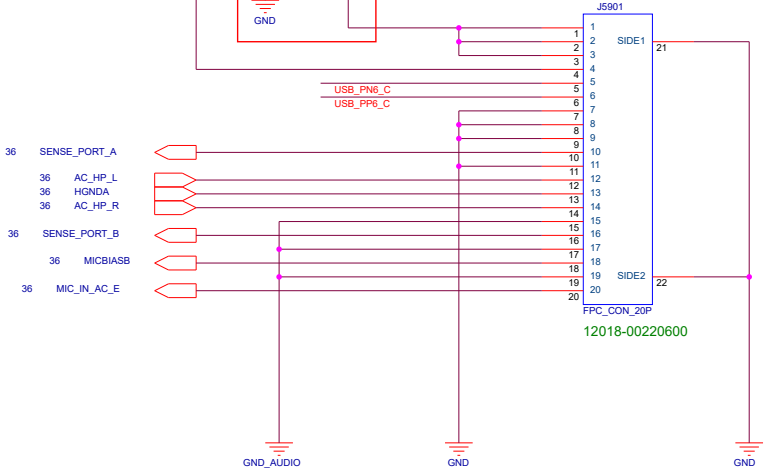
1st Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L <G>

2nd Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S <G>



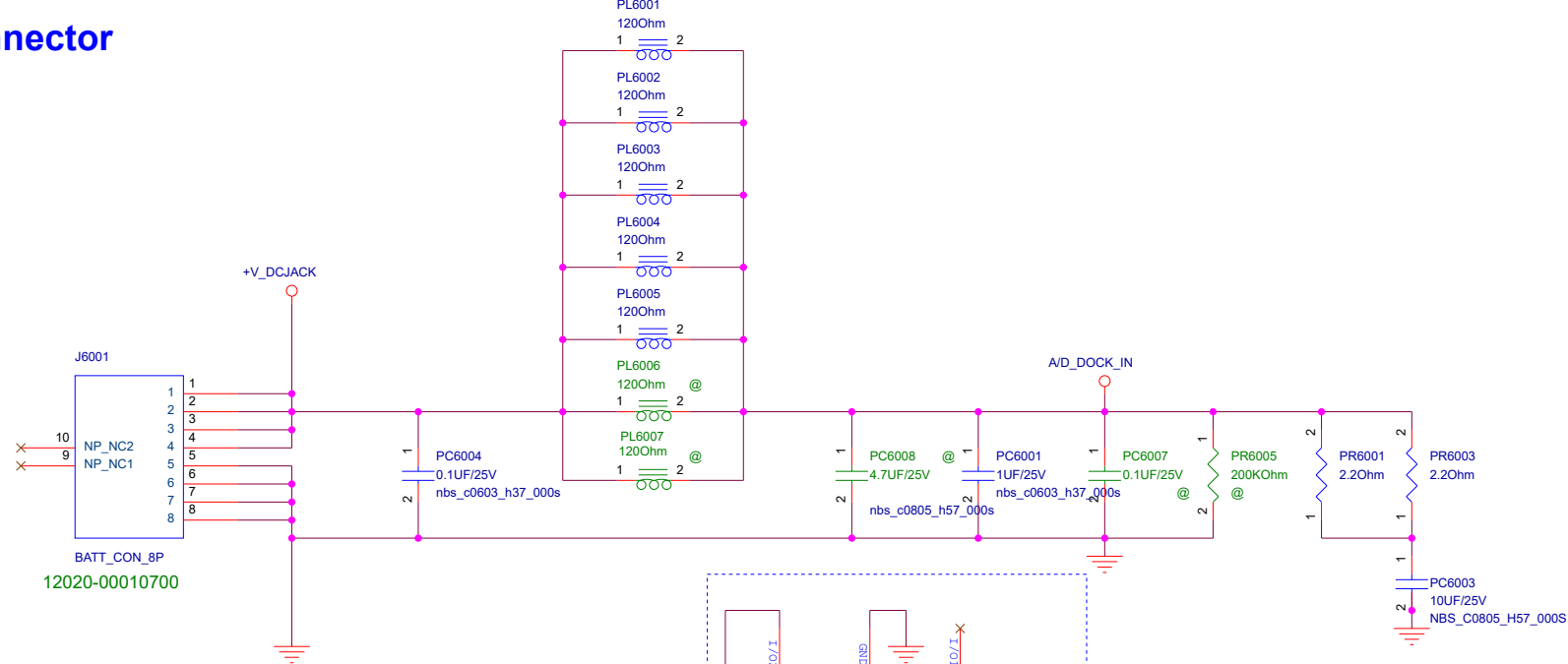
Close to connector for EMI

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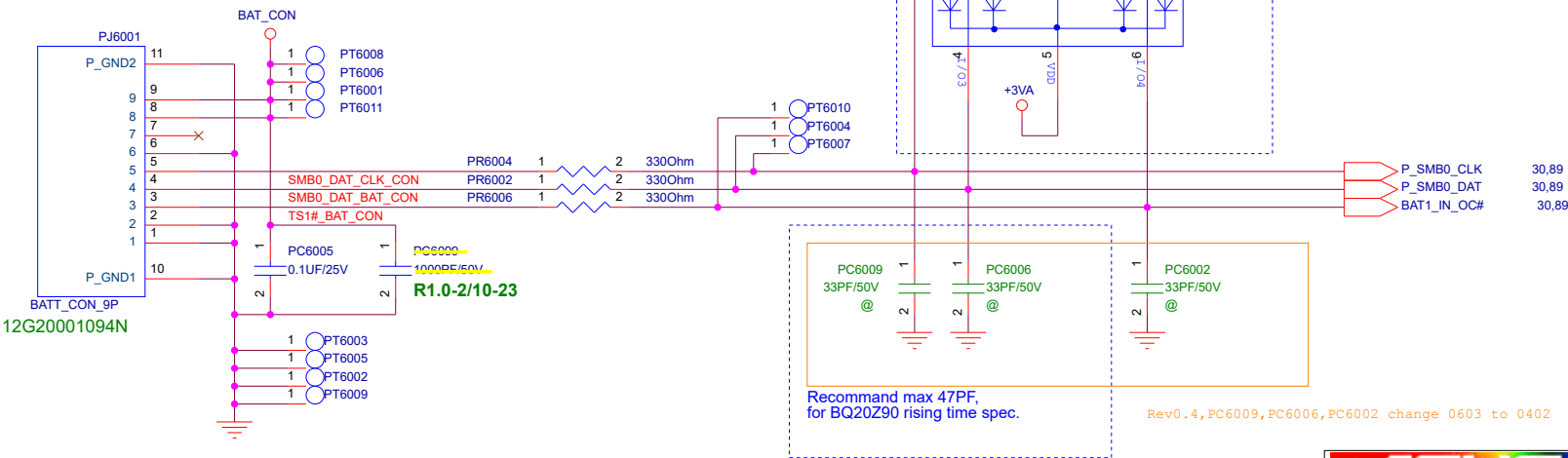


R1.1-5/11-3

DC-IN Connector



Battery Connector



081111 -> 090604:
1. Change PD6001 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.



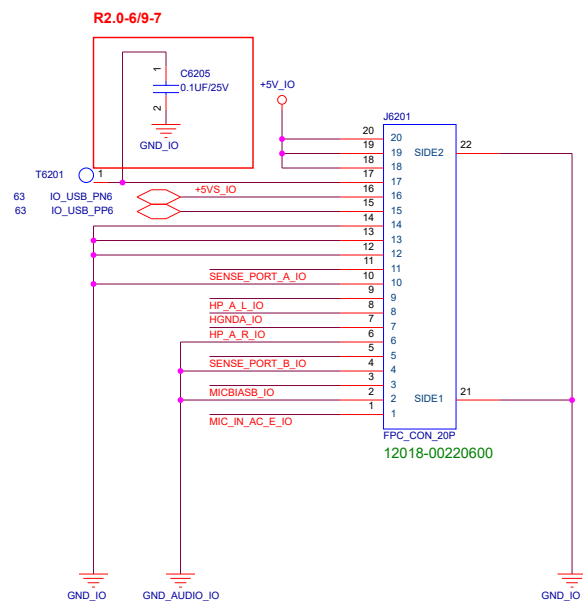
Title : BT_Bluetooth

ASUSTeK COMPUTER INC. NB1

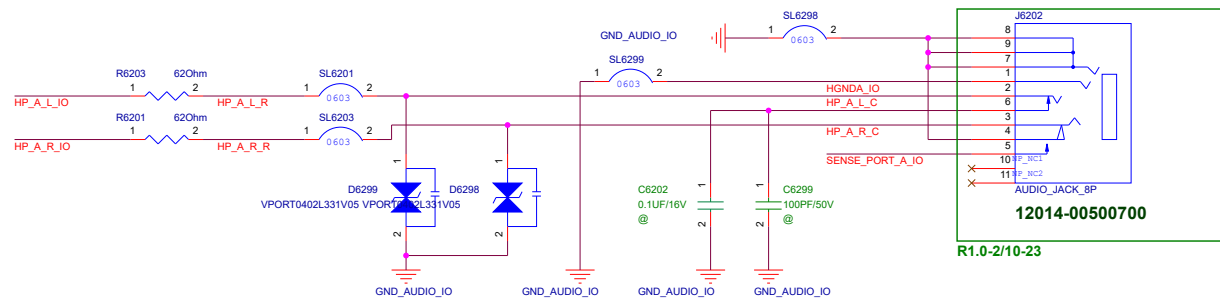
Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0

HP JACK for Dual JACK Solution



Change to 07g005000313 in
SR2 20141027



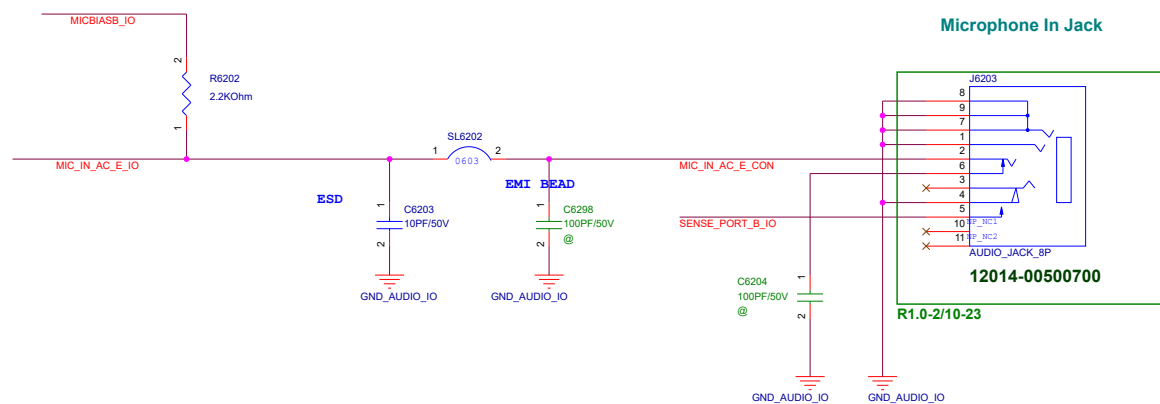
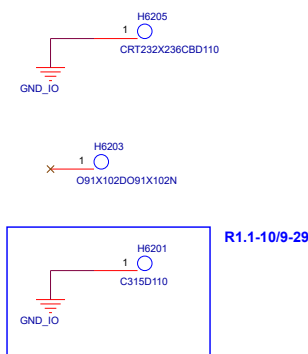
J6202,J6203 Audio Jack :

1st Source: P/N:12014-00500700 SINGATRON/2SJ3015-029111F

2nd Source: P/N:12014-00500800 SIMULA/AJ3D1A-Y200-422.

R1.0-5/10-27

EXTERNAL MICROPHONE

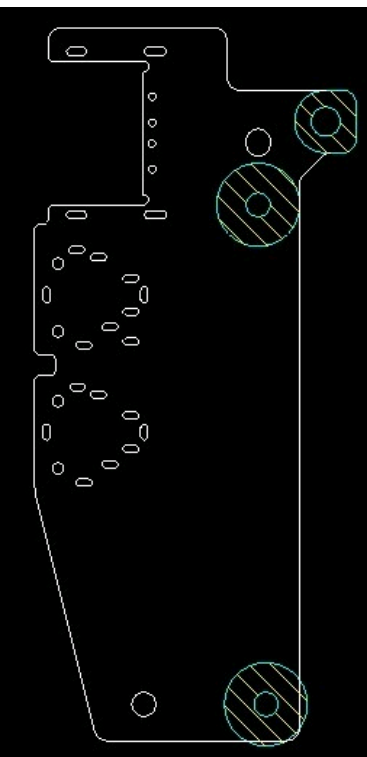
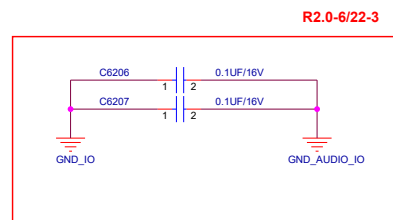


J6202,J6203 Audio Jack :

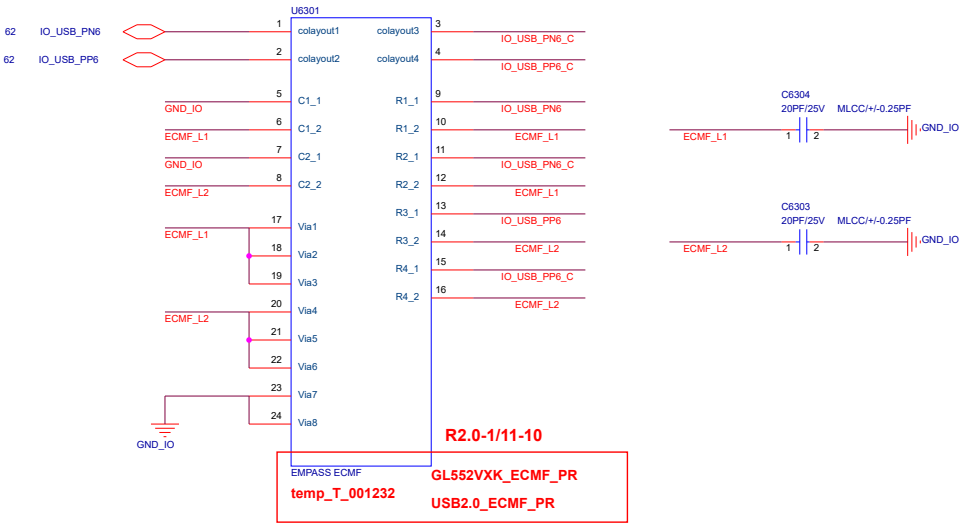
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2nd Source: P/N:12014-00500800 SIMULA/AJ3D1A-Y200-422.

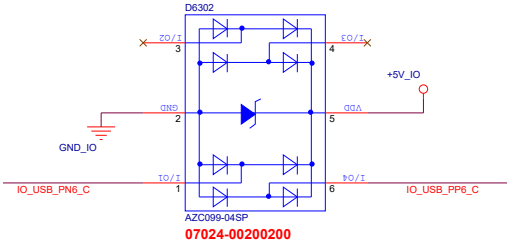
R1.0-5/10-27



USB2.0 Port 6 Embedded Common Mode Filter



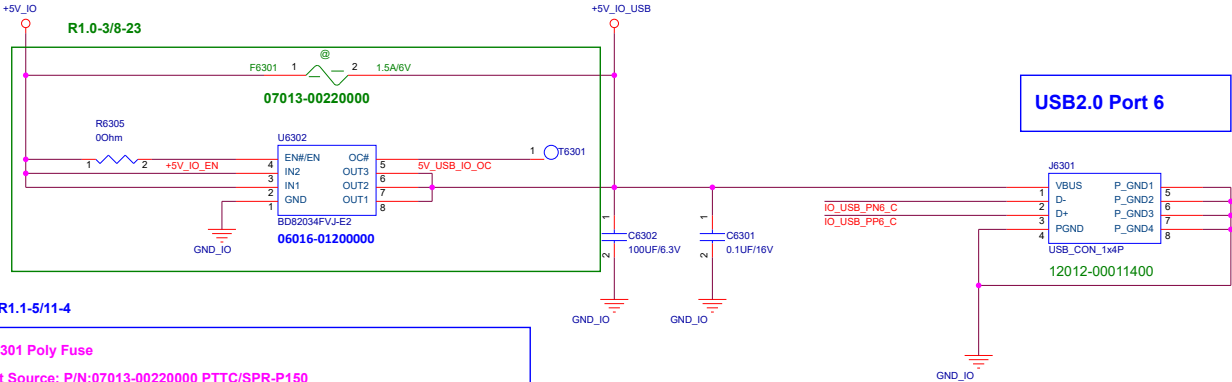
USB2.0 Port 6 ESD Protection



R2.0-6/11-08

D6302 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

USB2.0 Port 6 Power Protection & Type-A Connector



R1.1-5/11-4

F6301 Poly Fuse
1st Source: P/N:07013-00220000 PTT/SPR-P150
2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR



Title : I/O board(1-3)_USB

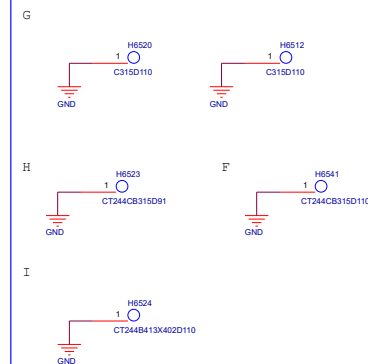
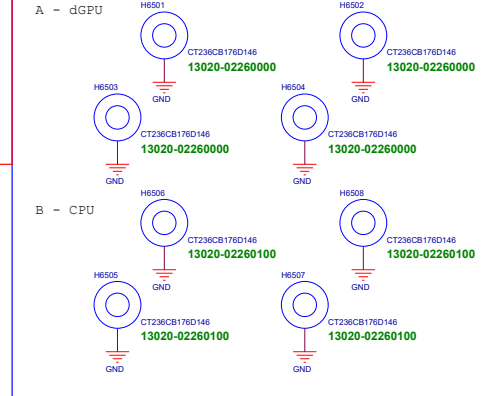
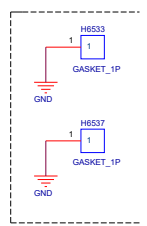
ASUSTeK COMPUTER INC. NB1

Engineer: Wenchi_Shen

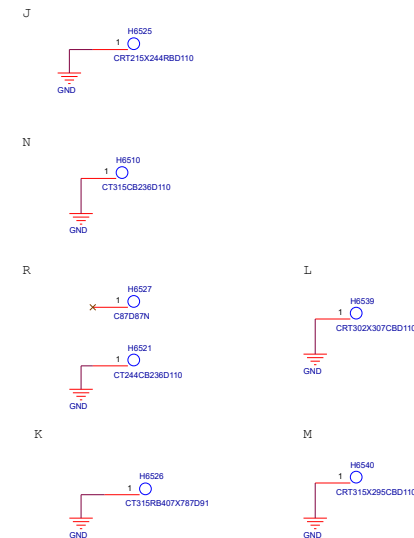
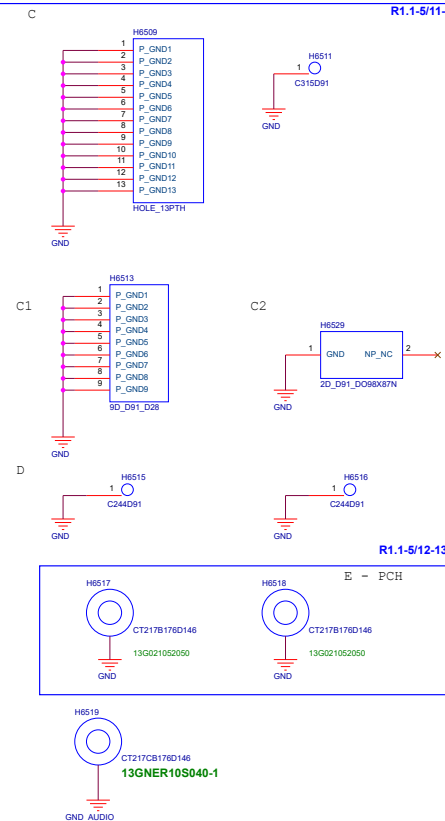
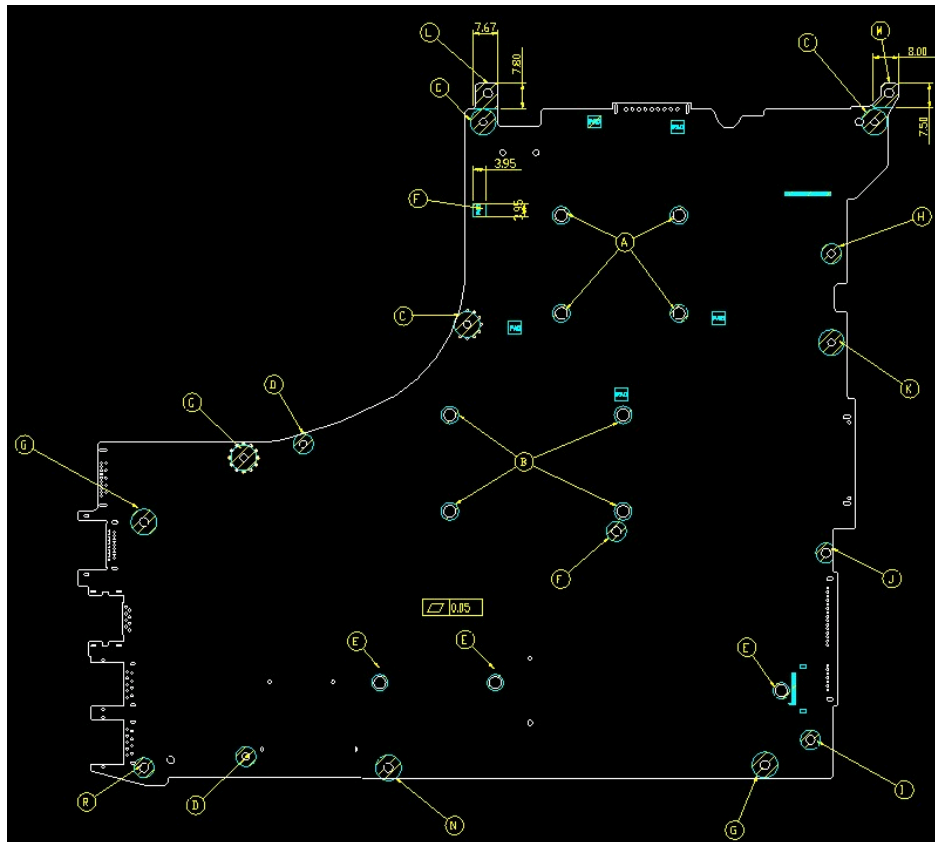
Size	Project Name	Rev
A	GL552VXK	2.0


Figure 1 shows seven circuit diagrams illustrating different ways to connect a 1 ohm resistor (R3) to ground. Each diagram features a 1 ohm resistor connected to a node labeled with a part number and a value of 1. The node is connected to ground (GND) through various components:

- H6530:** A 1 ohm resistor connected to a node labeled H6530 1. The node is connected to GND through a 1 ohm resistor labeled LPG-R-3-2-5-3.
- H6531:** A 1 ohm resistor connected to a node labeled H6531 1. The node is connected to GND through a 1 ohm resistor labeled LPG-R-3-2-5-3.
- H6532:** A 1 ohm resistor connected to a node labeled H6532 1. The node is connected to GND through a 1 ohm resistor labeled LPG-R-3-2-5-3.
- H653B:** A 1 ohm resistor connected to a node labeled H653B 1. The node is connected to GND through a 1 ohm resistor labeled GASKET_1F.
- H6534:** A 1 ohm resistor connected to a node labeled H6534 1. The node is connected to GND through a 1 ohm resistor labeled LPG-R-3-2-5-3.
- H6535:** A 1 ohm resistor connected to a node labeled H6535 1. The node is connected to GND through a 1 ohm resistor labeled LPG-R-3-2-5-3.
- H6536:** A 1 ohm resistor connected to a node labeled H6536 1. The node is connected to GND through a 1 ohm resistor labeled LPG-R-3-2-5-3.



H6533 & H6537 Change to H=3.5mm Gasket in PR



		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: Wenchi_Shen	
Size	Project Name		Rev
A	GL552VXX		2.0
Date:	Thursday, November 10, 2016	Sheet	66 of 103



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: **Wenchi_Shen**

Size	Project Name	Rev
A	GL552VXK	2.0

Date: **Thursday, November 10, 2016**

Sheet **67** of **103**



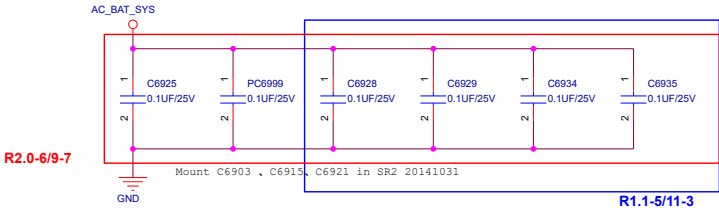
Title : OTH_for test only

ASUSTeK COMPUTER INC. NB1

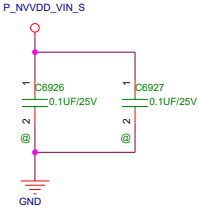
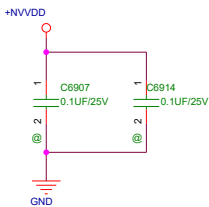
Engineer: Wenchi_Shen

Size	Project Name	Rev
A	GL552VXK	2.0

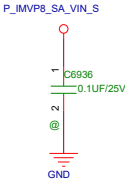
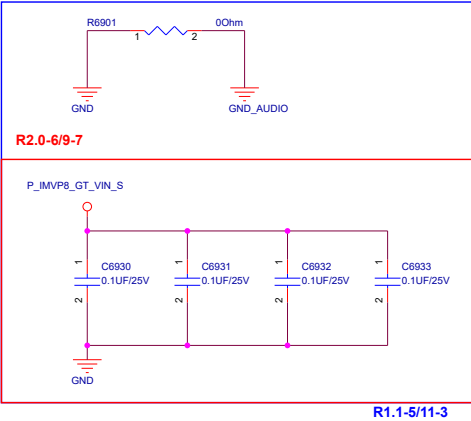
2014-02-12 Add EMI solution
(6042.00 6728.00)、(1947.00 3850.00)、
(1757.00 1852.00)、(6369.00 -299.00)



(6490.00 4706.00)、(7437.00 3852.00)

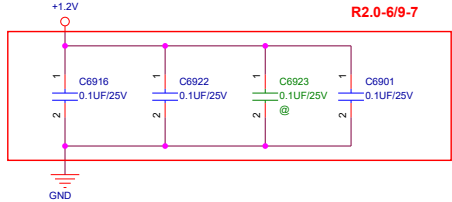


(8004.00 585.00)



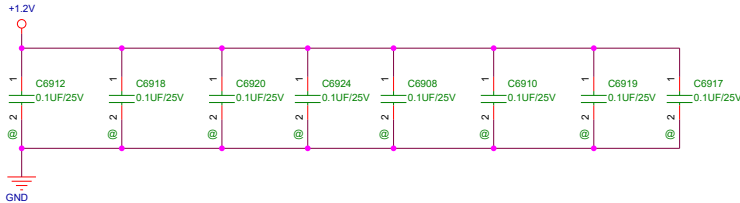
R1.0-16

2014-04-03 Add EMI solution
(3678, 2622)、(4011, 2594)、(4975, 2580)、(5169, 2585)

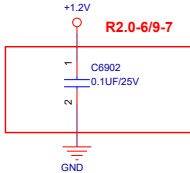


R1.1-15
R1.1-24

2014-04-03 Add EMI solution
Top
(3541,2591)、(3339,2115)、(3807,2452)、(4030,2118)、
(3367,1670)、(3583,1965)、(3819,1953)、(4013,1650)



Bot (3809, 2558)



R1.1-22
R1.1-24

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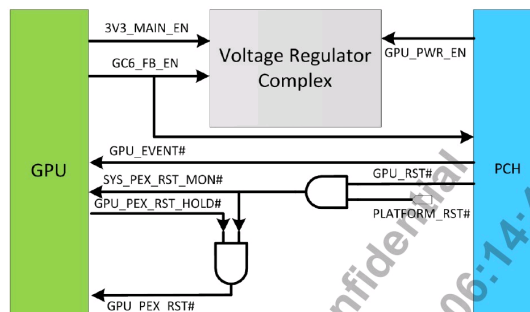
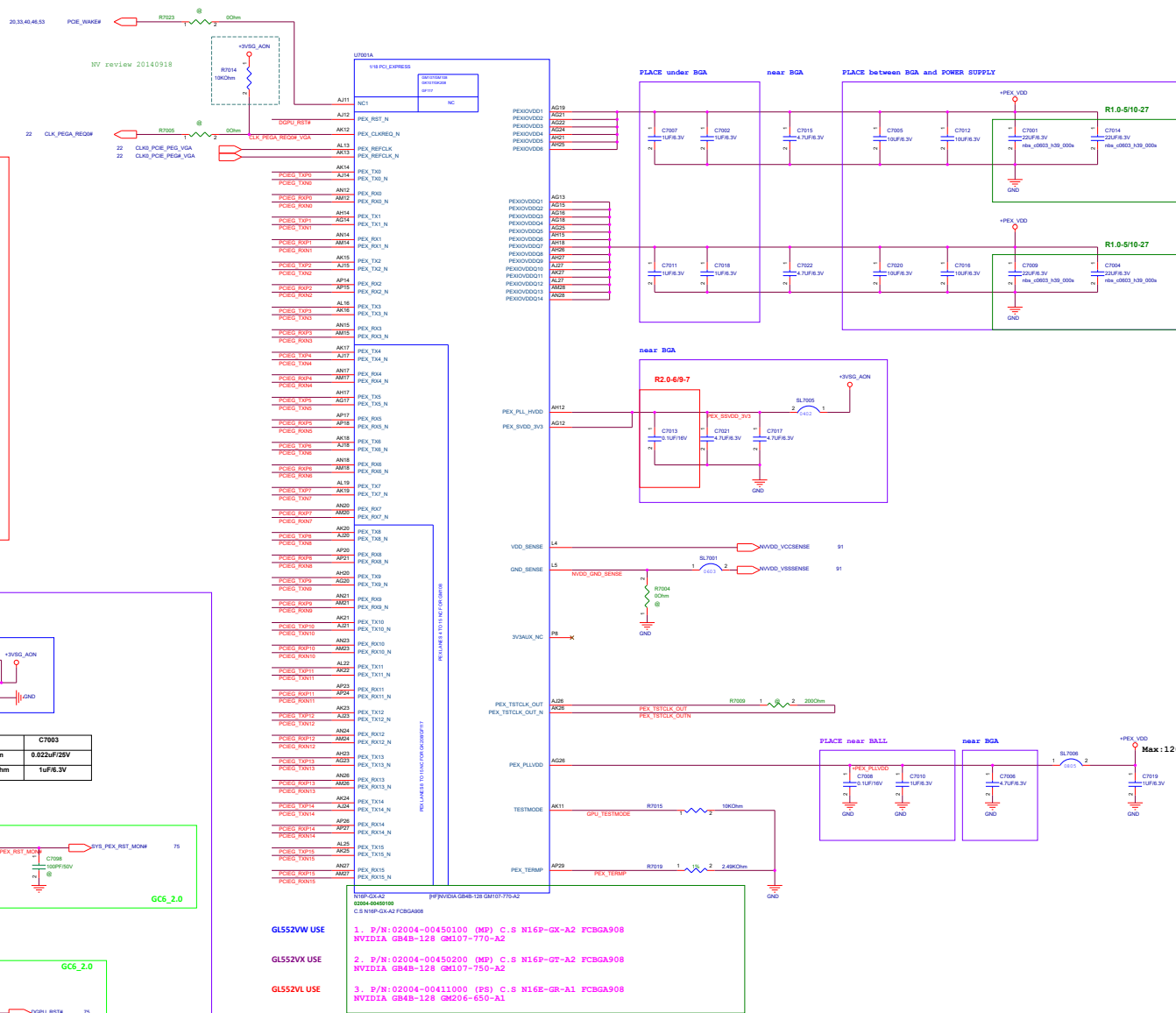
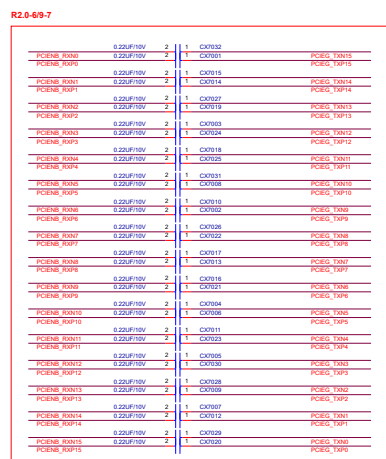


Figure 18-9. GC6 2.0 High-level Signal Connection Concept

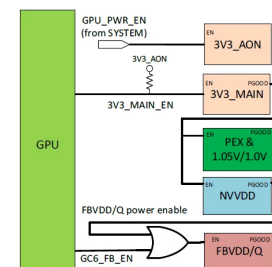
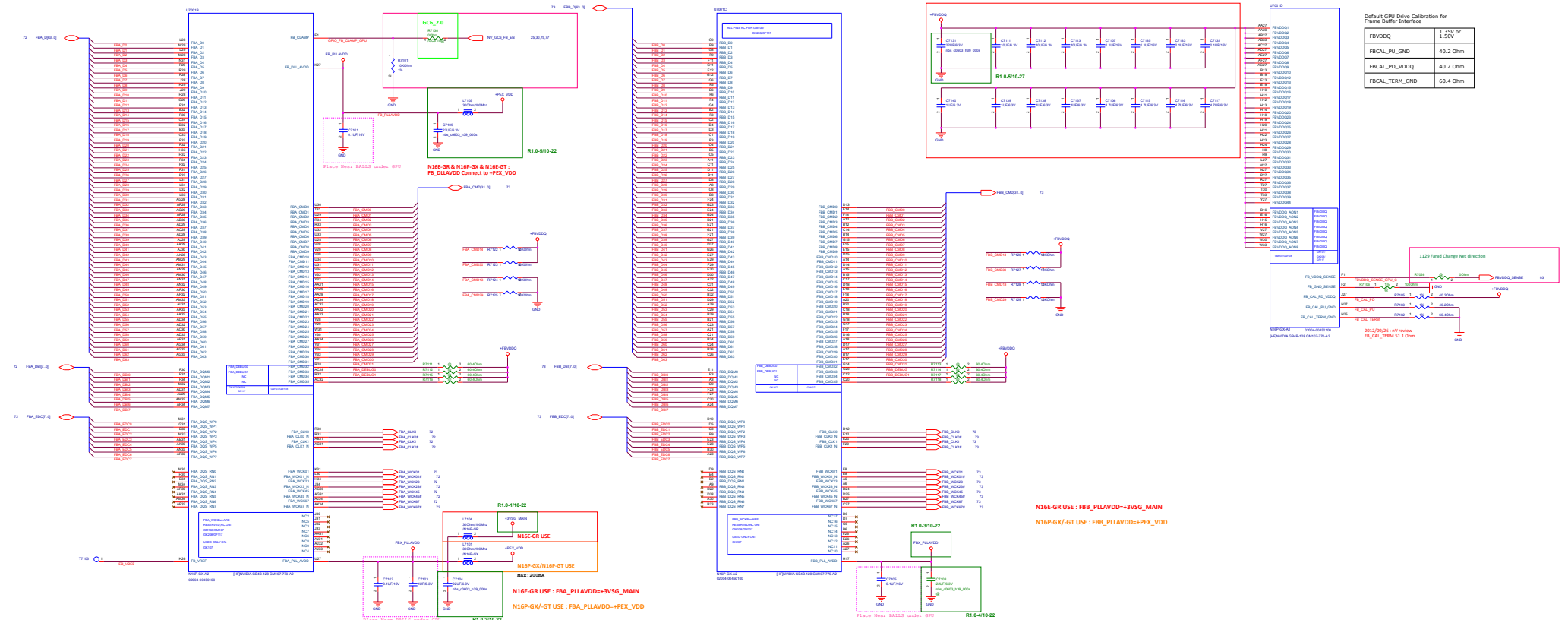
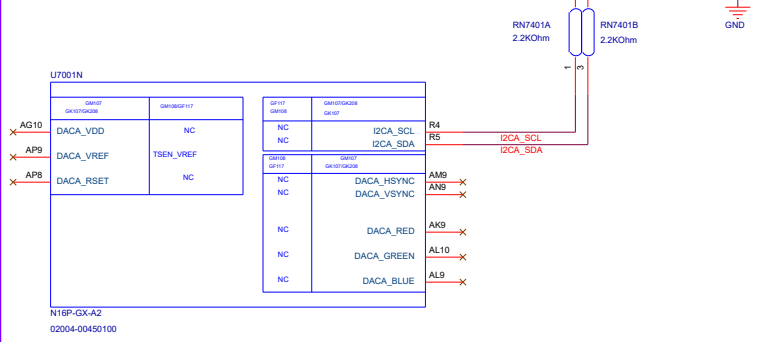


Figure 18-8. GC6 2.0 Voltage Regulator Complex Signal Connection

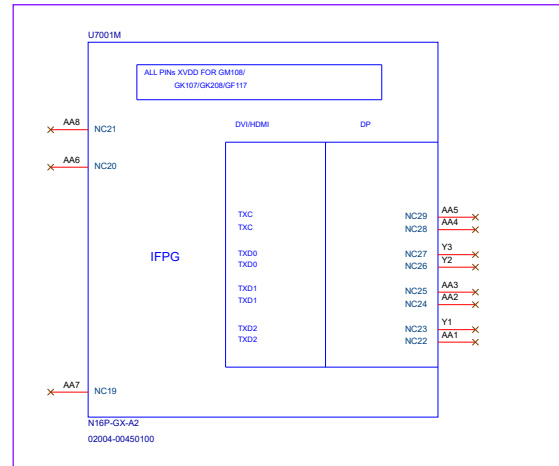


CRT DAC_A

DG-06246-001_v04 DG9.6 p170
DAC interface not used
Leave DACA_VDD floating
All Other pin (DACA_VREF,DACA_RSET) NC

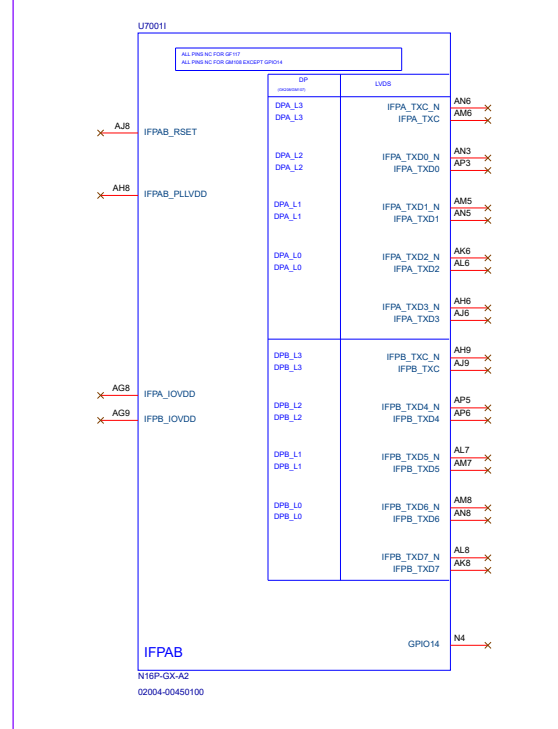


LVDS IFPG

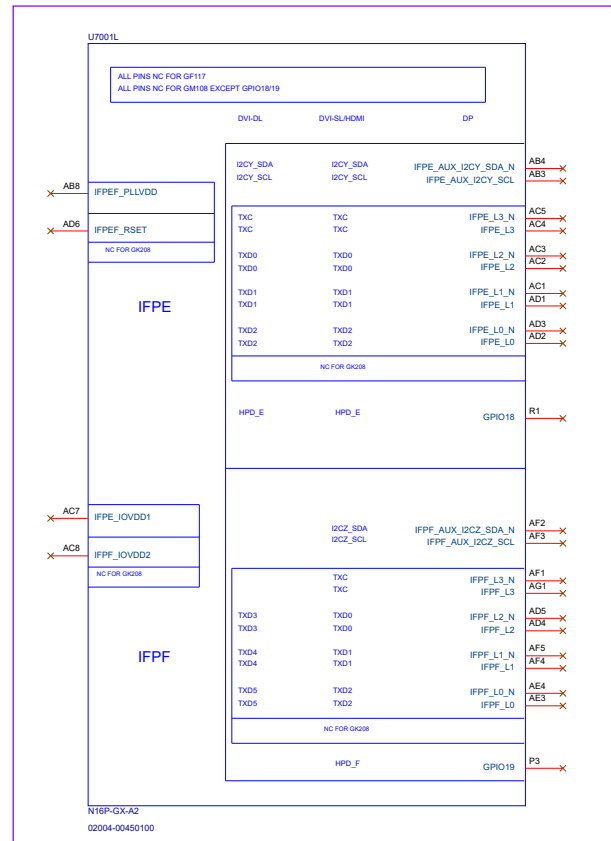


LVDS IFPA/B

DG-06246-001_v04 DG8.6 p162
Float IFPxy_IOCDD/IFPxy_PLLVDD
Other pin NC



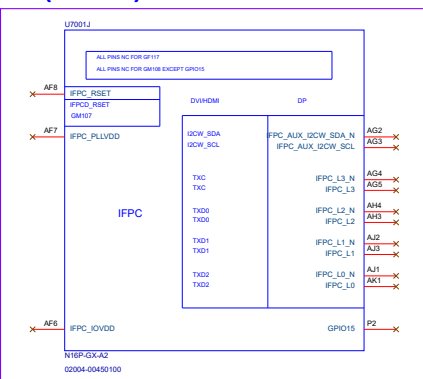
LVDS IFPE/F



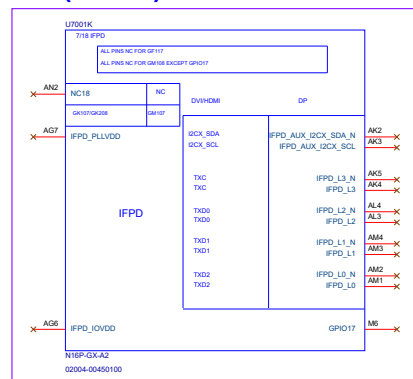
GPIO ASSIGNMENTS

DG-06246-001_v02 p157 DG8.6
 IPF not used
 IFPxy_IOCDD/IFPxy_PLLVDD 10K PD
 Other pin NC

DP(link C)



DVI(link D)

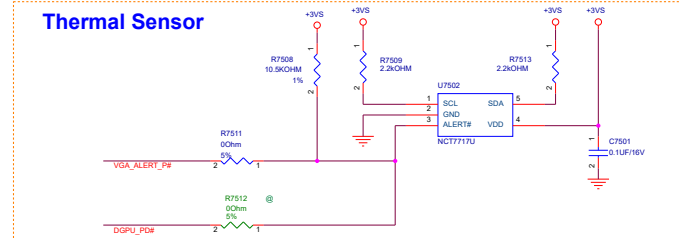


GPIO ASSIGNMENTS

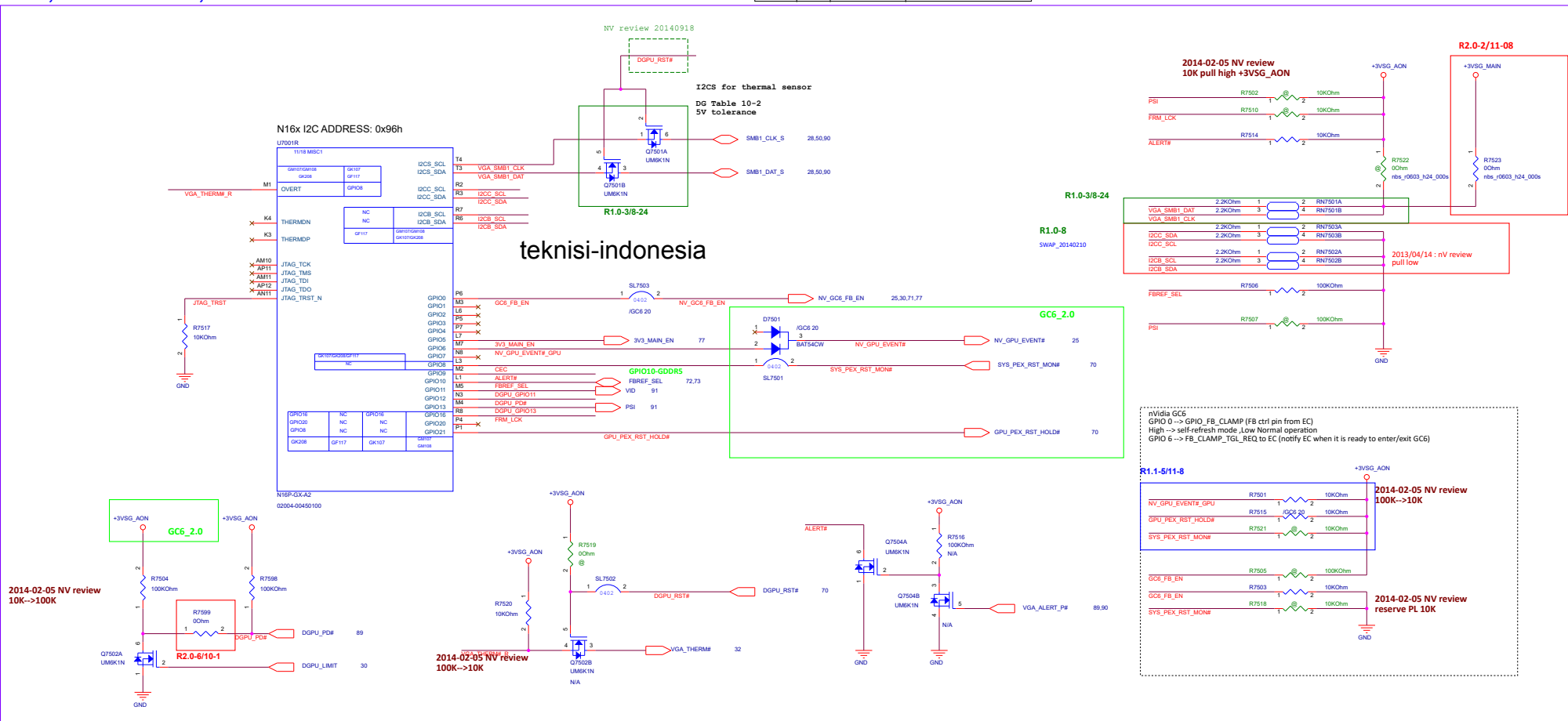
GPIO	I/O	ACTIVE	USAGE
0	OUT	Low	GC6_FBEN
1	OUT	High/Low	MEM_VDD_CTL
2	OUT	Low	LCD_BL_FWM
3	OUT	Low	LCD_VCC
4	OUT	Low	LCD_BLEN
5	OUT	High	3V3_MAIN_EN
6	IN	High	GPU_EVENT#
7	OUT	Low	3Dvision
8	IN	High	SYS_PEX_RST_MON#
9	I/O	High	THERM_ALERT
10	OUT	Low	MEM_VREF_CTL
11	OUT		PWM_VID
12	IN	High	PWR_LEVEL
13	OUT	High	PSI
14	IN	Fig. 12-1	HPD_IFFAB
15	IN	Fig. 12-1	HPD_IFFC
16	IN	High	FRAME_LOCK#
17	IN	Fig. 12-1	HPF_IFFD
18	IN	Fig. 12-1	HPD_IFFE
19	IN	Fig. 12-1	HPD_IFFFB
20			Reserved
21	OUT	High	GPU_PEX_RST_HOLD#
OVERT	I/O	High	OVERT

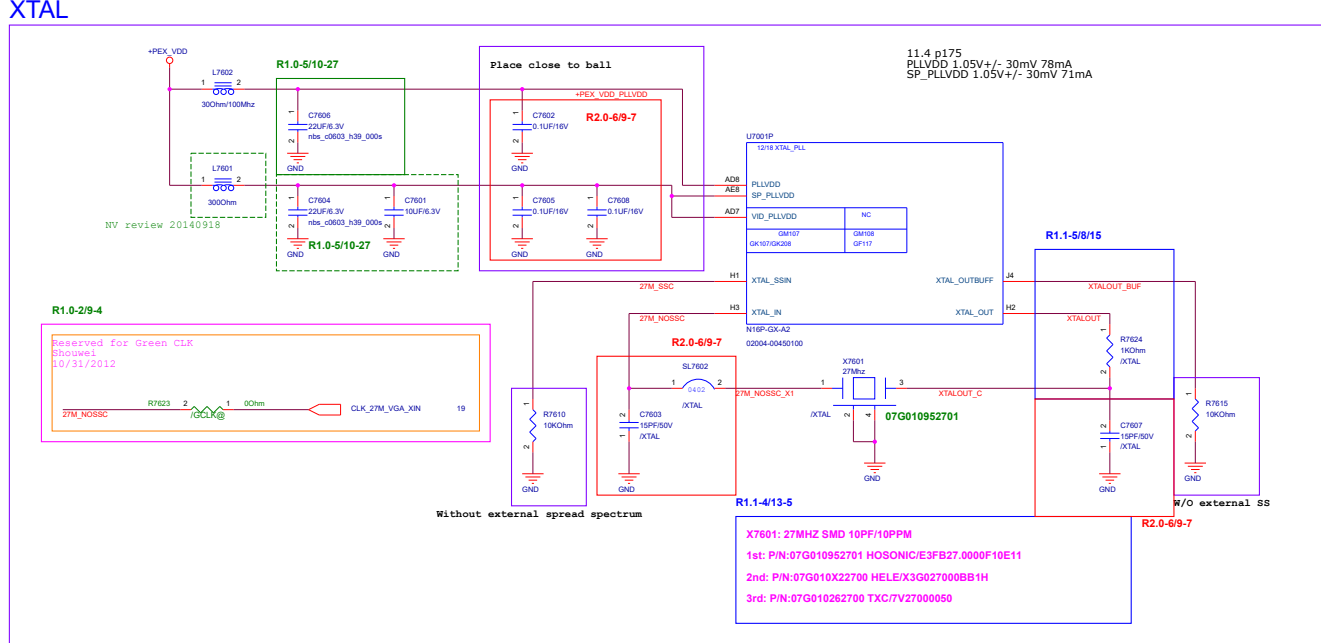
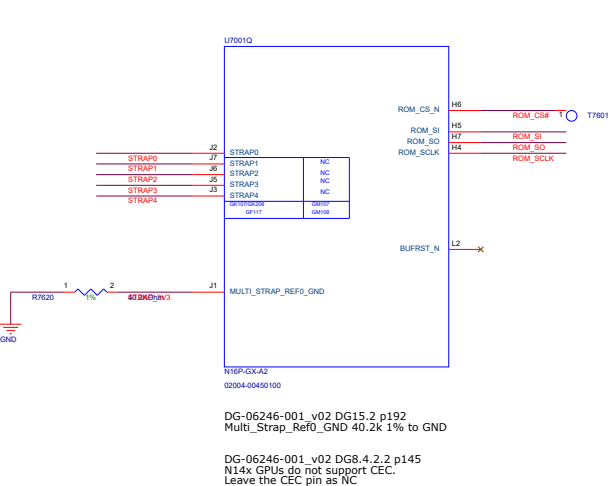
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Thermal Sensor

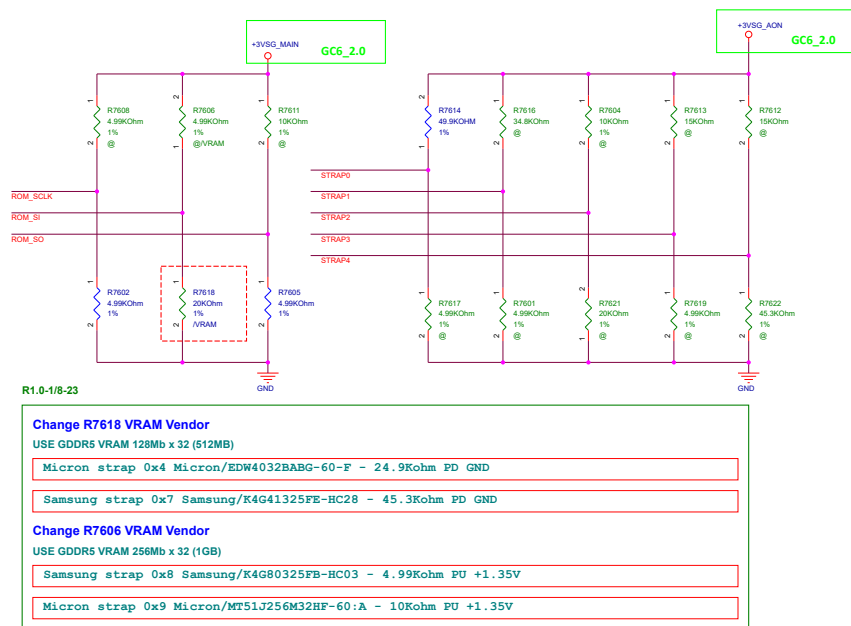


GPIO, TEMP SENSOR, JTAG





STRAPPING OPTIONS for N16P



DG-07158-001_v05_secured p.197
Table 15-3. GB48-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 40.9 kohm pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not Stuff.			
STRAP2				
STRAP3				
STRAP4				

Table 15-2.

PU	PD
4.99Kohm	1000 0000
10.0Kohm	1001 0001
15.0Kohm	1010 0010
20.0Kohm	1011 0011
24.9Kohm	1100 0100
30.1Kohm	1101 0101
34.8Kohm	1110 0110
45.3Kohm	1111 0111

FBVDDQ	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

N16P-GX/-GT GDDR5 MEMORY RVL

RVL-07229-001_v19-1000044-08

NVIDIA recommends the following GDDR5 memories for use in conjunction with notebook designs using N16P-GX/-GT GPUs.

Table 7. N16P-GX/-GT GDDR5 Recommended Memories

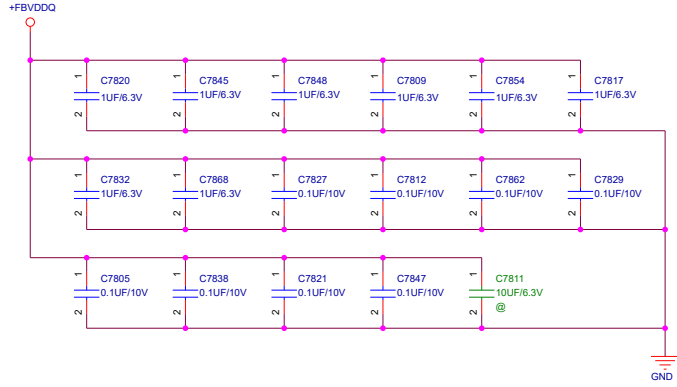
Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GC4H24BFR-T2C	B-die	0x1	2500	N/A	Production ready
			Micron	EDW20128B8G-6A-F	B-die	0x5	2500	N/A	Production ready
			Samsung	K4G0325FD-FC03	D-die	0x0	2500	N/A	Production ready
			Micron	EDW4032BAG-60-F	A-die	0x4	2500	N/A	Production ready
		256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24BFR-T2C	M-die	0x2	2500	N/A	Production ready
			Hynix	H5GC4H24BFR-T2C	A-die	0x6	2500	N/A	Post production ready
		128Mx32	Micron	EDW4032BAG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24BFR-T2C	M-die	0x2	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x8	2500	N/A	Post production ready
			Hynix	H5GC4H24BFR-T2C	M-die	0x4	2500	N/A	Post production ready
			Micron	MT51J256M32HF-60-A	A-die	0x9	2500	N/A	Post production ready

- Note:
- For N16P-GX/-GT, the maximum allowable memory case temperature is 85 °C.
 - 8 Gb is supported in >32 configuration only (no >16 support planned).

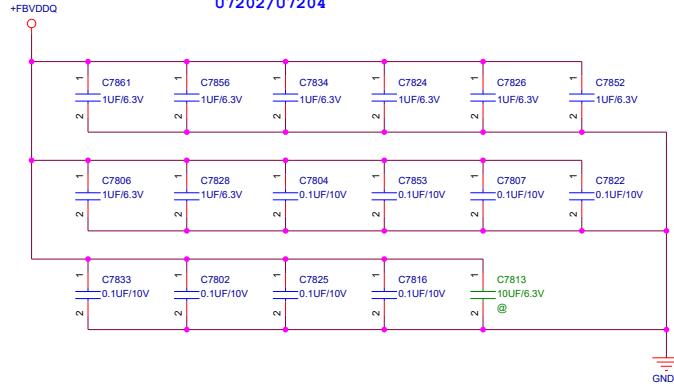
Location is close to DRAM for clamshell mode

0.1uF X8
1uF X 8

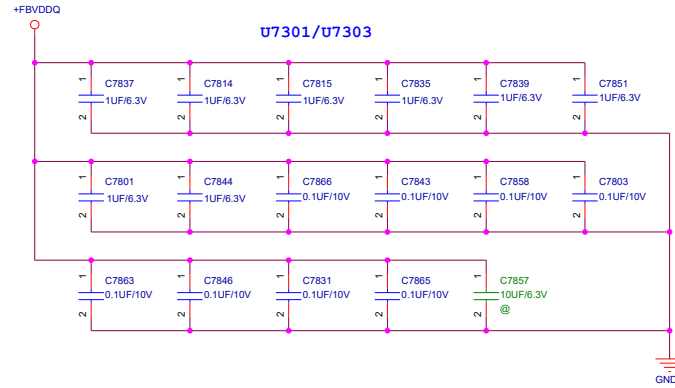
U7201/U7203



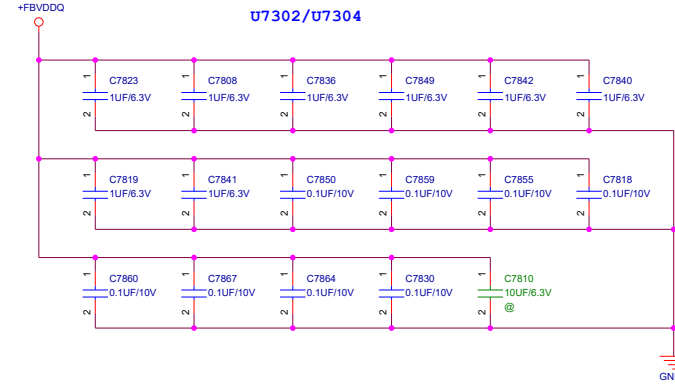
U7202/U7204



U7301/U7303



U7302/U7304





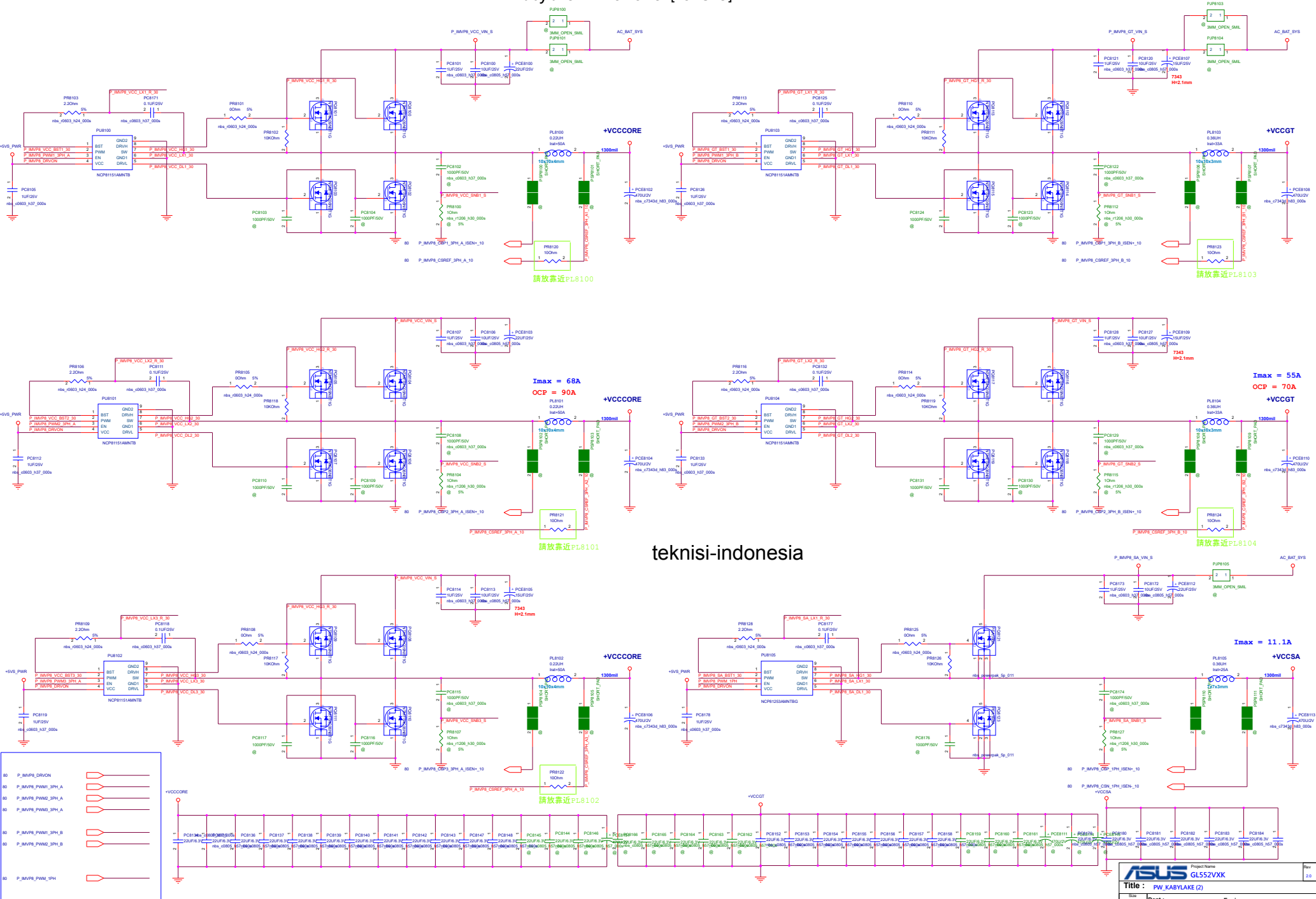
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ASUSTeK COMPUTER INC. NB1

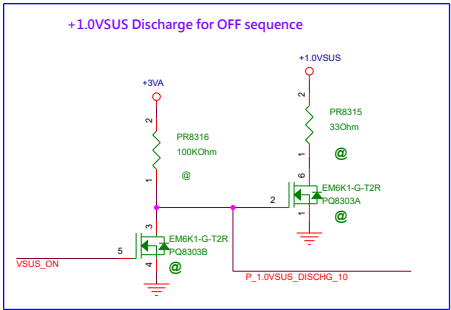
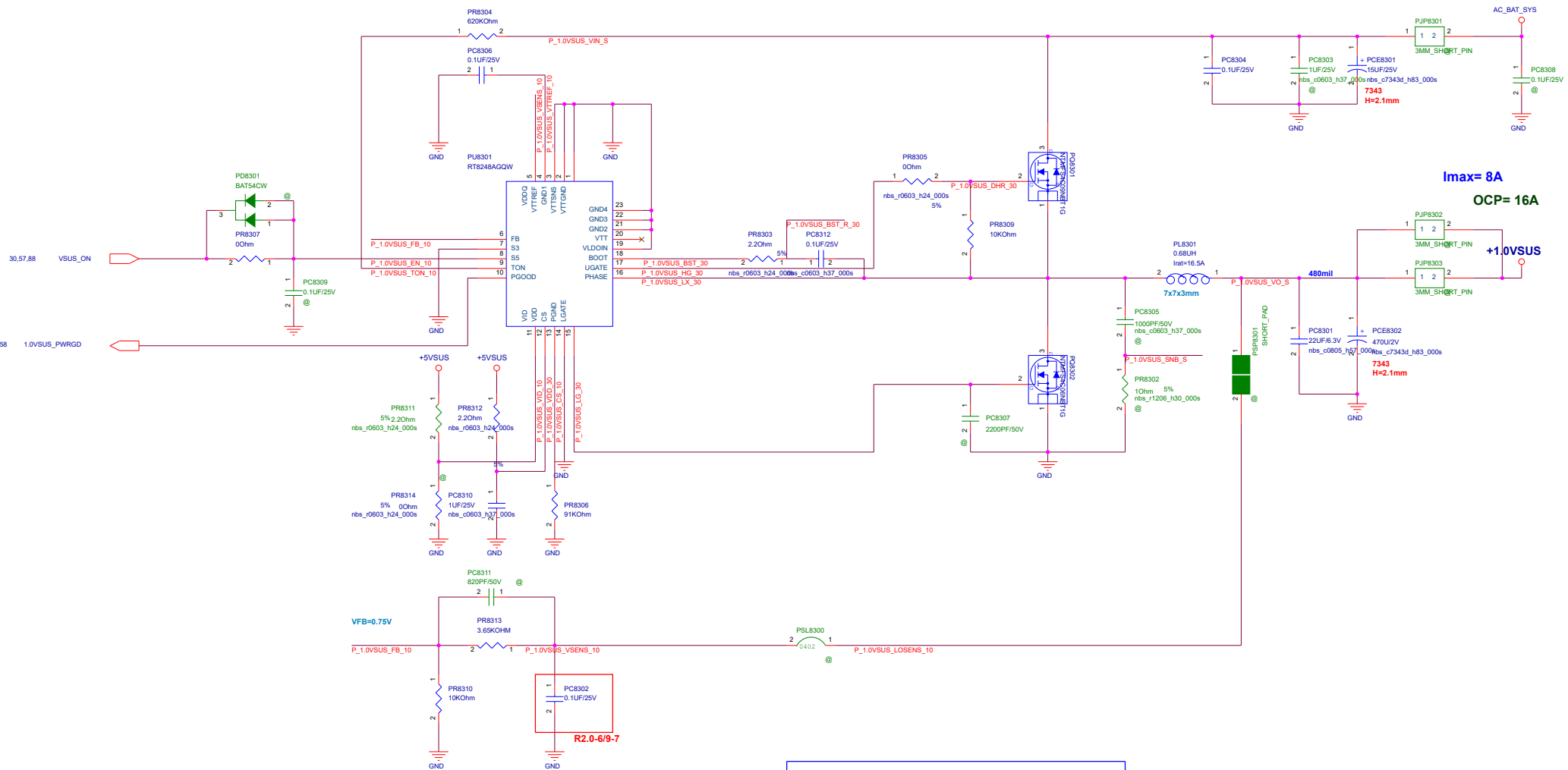
Engineer: Wenchi_Shen

Size	Project Name	Rev
C	GL552VXK	2.0

Kabylake IMPV8 Power [For CPU]



+1.0VSUS [For PCH]



+VCCIO [For CPU]





Project Name

GL552VXX

Rev

2.0

Title : POWER_+VGFX_CORE

Size

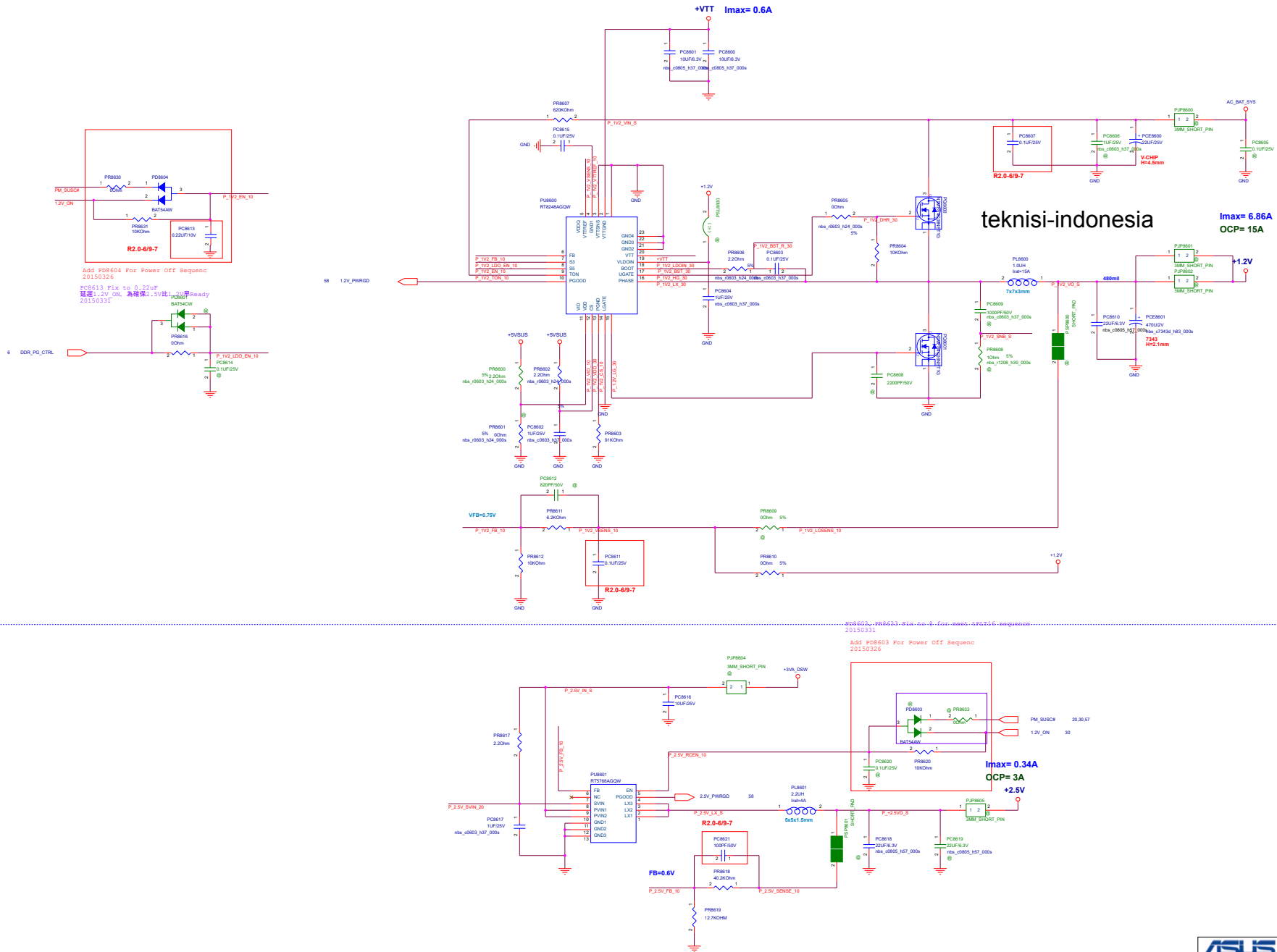
Custom

Dept.: ASUS&K COMPUTER INC. Engineer: Edison

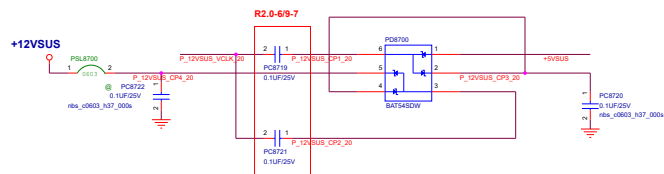
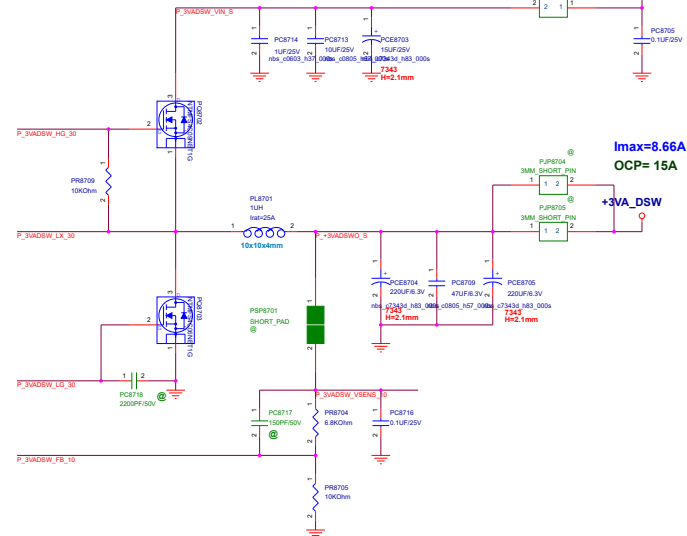
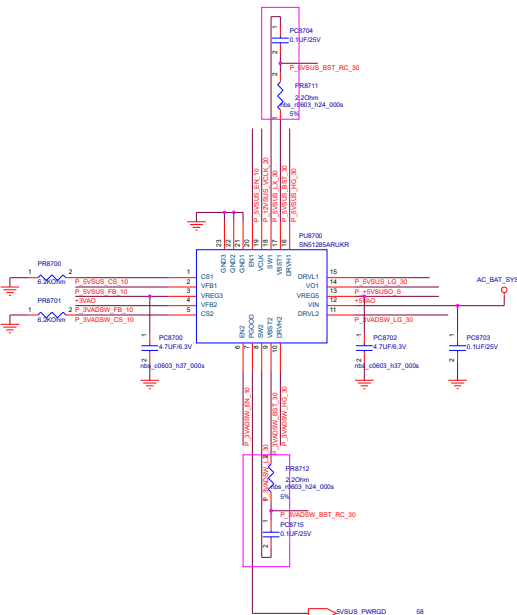
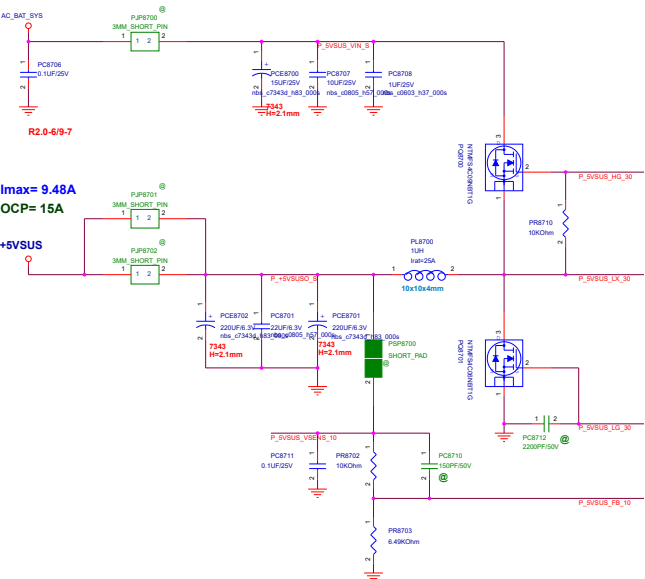
Date: Thursday, November 10, 2016

Sheet: 65 of 103

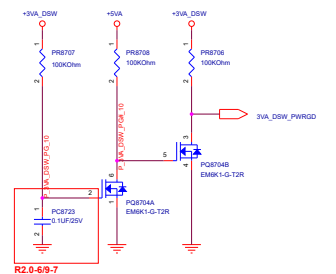
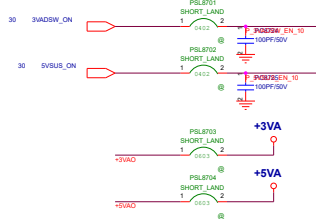
+1.2V / VTT / 2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]

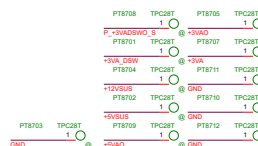


請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



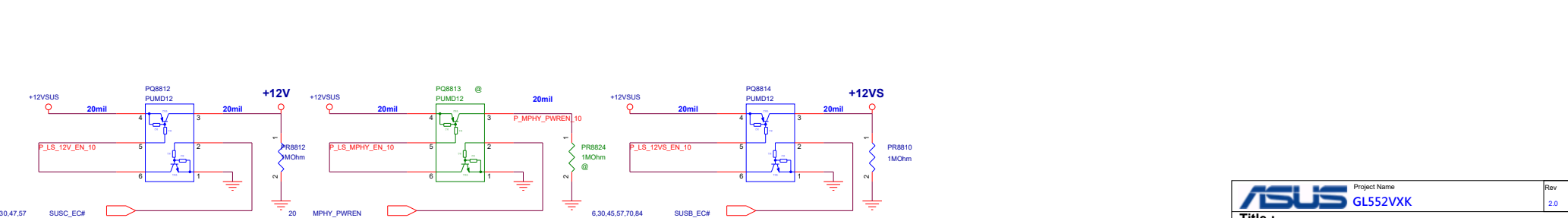
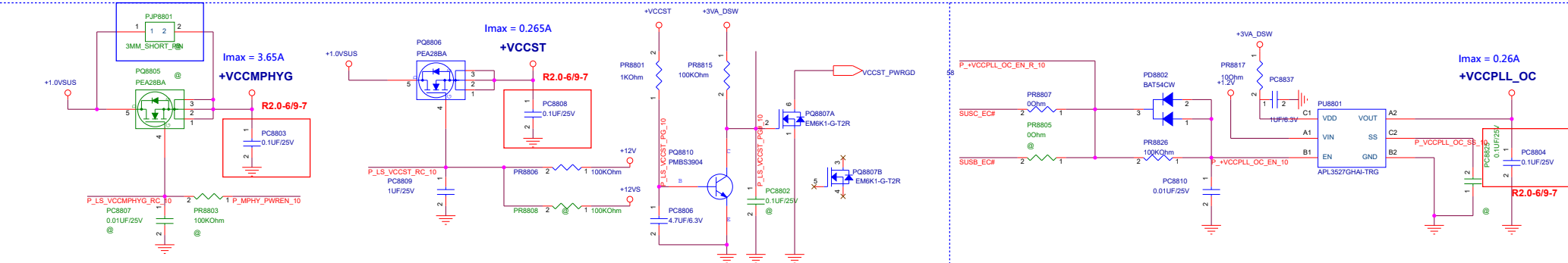
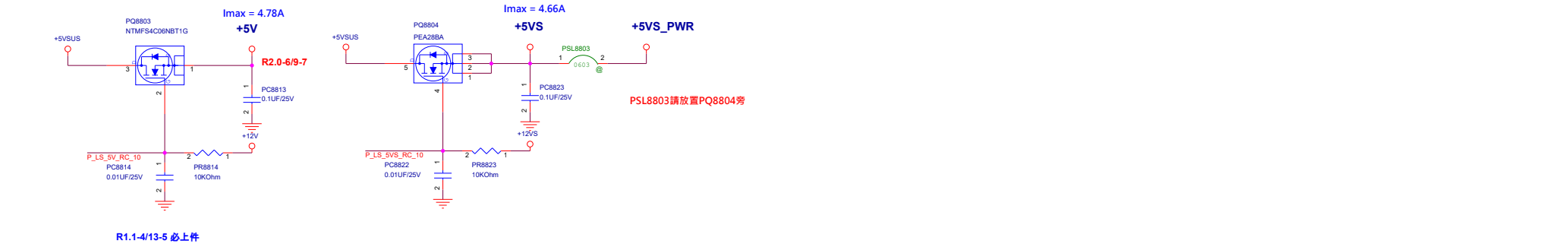
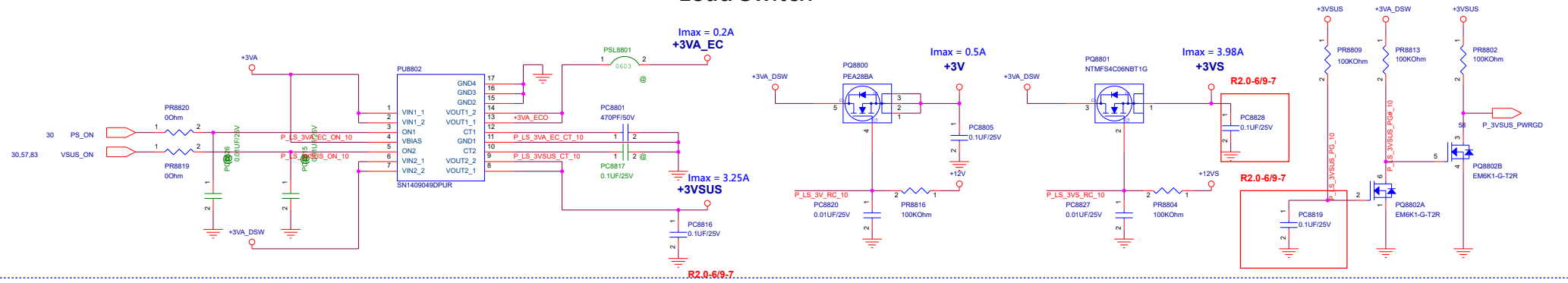
Adaptor Mode (MVP6)									
	S0	S3	S4	S5	S6	S7	S8	S9	S10
PS_ON	1	-	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	0	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	0	-	0	-	0	-	0

Battery Mode (MVP6)									
	S0	S3	S4	S5	S6	S7	S8	S9	S10
PS_ON	1	-	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	0	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	0	-	0	-	0	-	0



Load Switch

Main Board



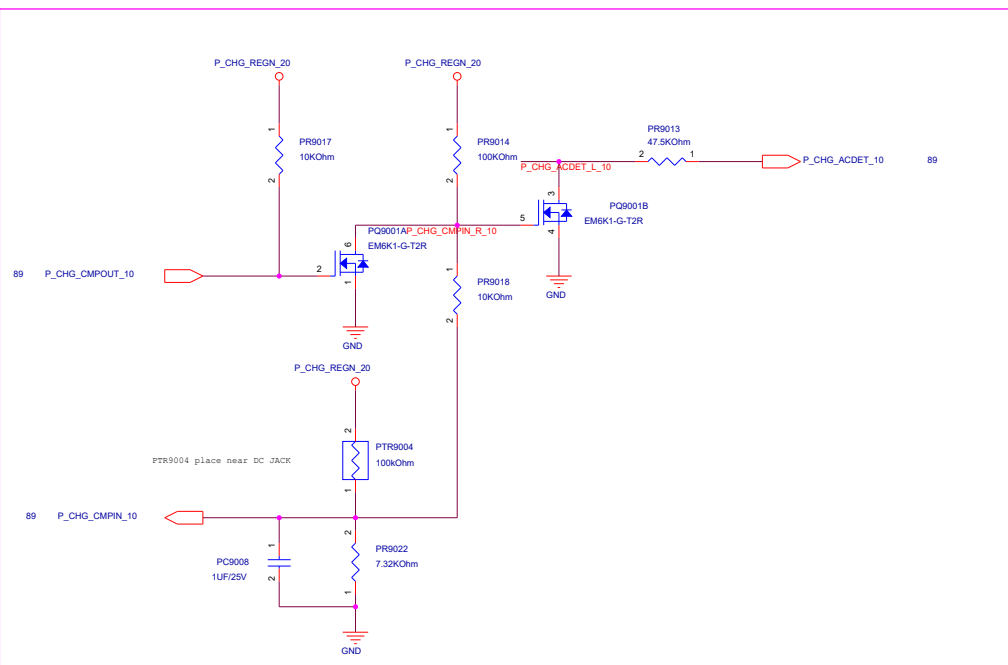
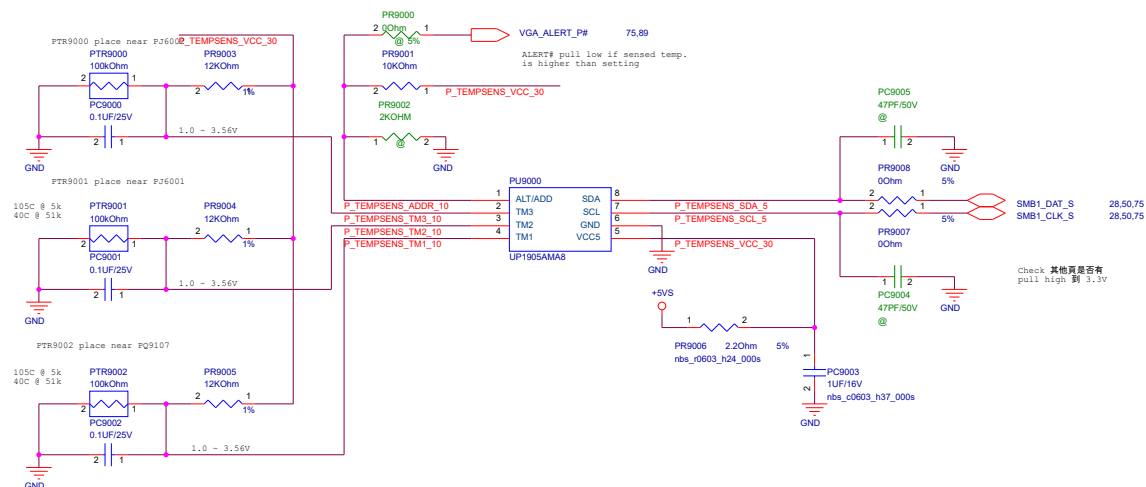
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9404	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9405	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

main body

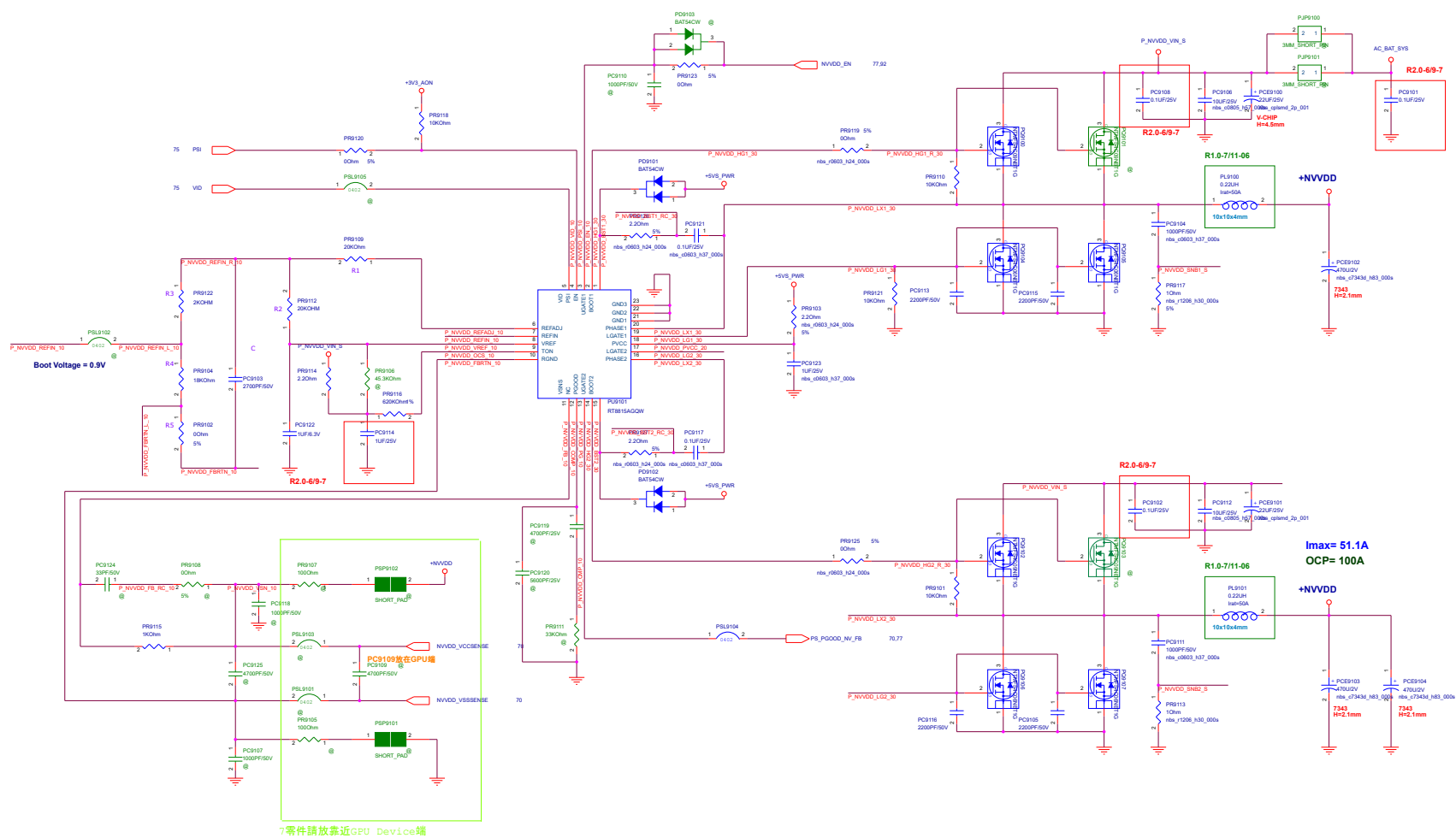
PTR9001 place near PQ8902
BAT_CON (PJ6001)

PTR9002 place near PQ9104
DGPU_NVDD PWR



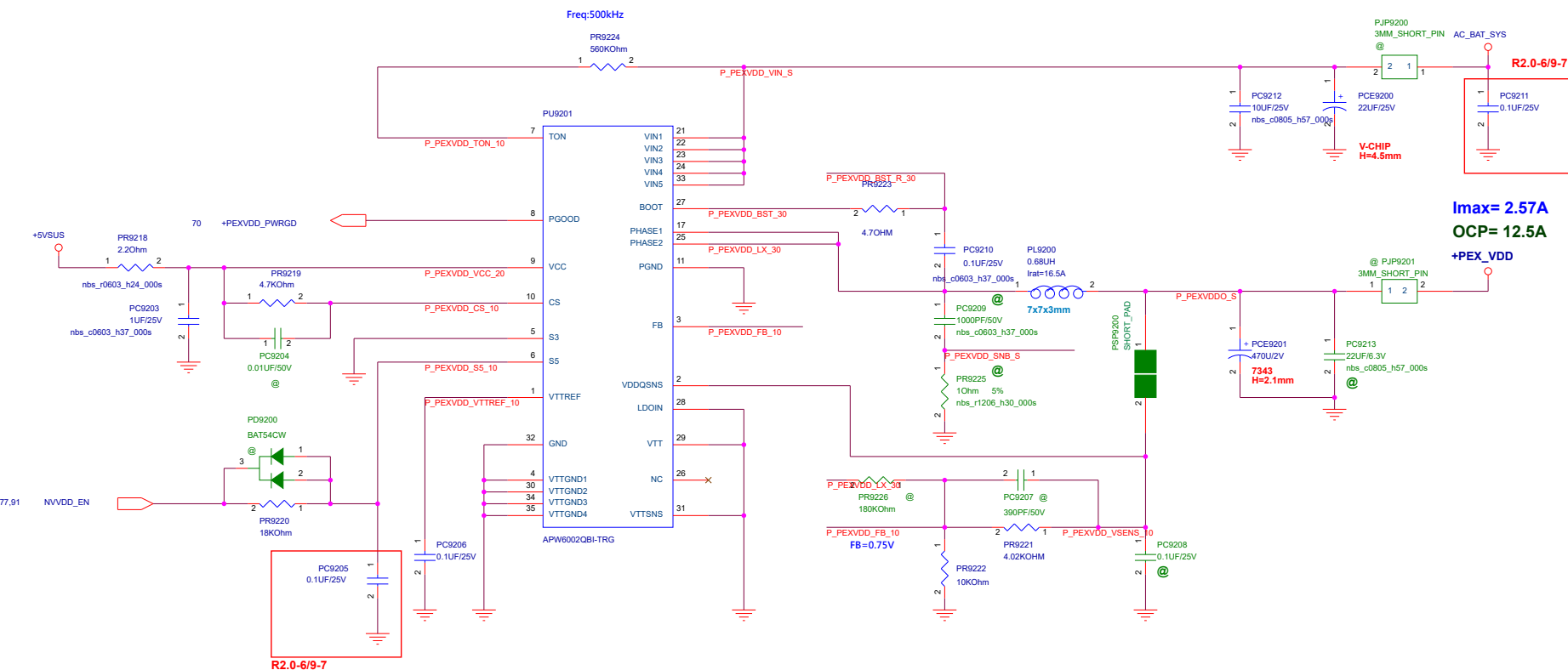
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+NVVDD [For DGPU]





	Config A	Config B
R1 (kohan)	39	20
R2 (kohan)	39	20
R3 (kohan)	1.5	2
R4 (kohan)	30	18
R5 (kohan)	1.5	0
C (nF)	1.5	2.7


+PEX_VDD [For DGPU]




PR9221	UP1740Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

		Project Name	Rev
		GL552VXK	2.0
Title :			
Size			
B	Dept.:	ASUSTeK COMPUTER INC. En	Engineer: Edison
Date:	Thursday, November 10, 2016	Sheet	94 of 103

		Project Name	Rev
		GL552VXK	2.0
Title :			
Size			
B	Dept.:	ASUSTeK COMPUTER INC. En	Engineer: Edison
Date:	Thursday, November 10, 2016	Sheet	95 of 103

		Project Name	Rev
		GL552VXK	2.0
Title :			
Size			
B	Dept.:	ASUSTeK COMPUTER INC. Edison	Engineer: Edison
Date:	Thursday, November 10, 2016	Sheet	96 of 103

Main Board

		Project Name	Rev
		GL552VXK	2.0
Title :			
Size			
A	Dept.:	ASUSTeK COMPUTER INC. USA	Engineer: Edison
Date:	Thursday, November 10, 2016	Sheet	97 of 103



Project Name

GL552VXX

Rev

2.0

Title :

Size

Custom

Dept.:

ASUSTeK COMPUTER INC.

Engineer:

Edison

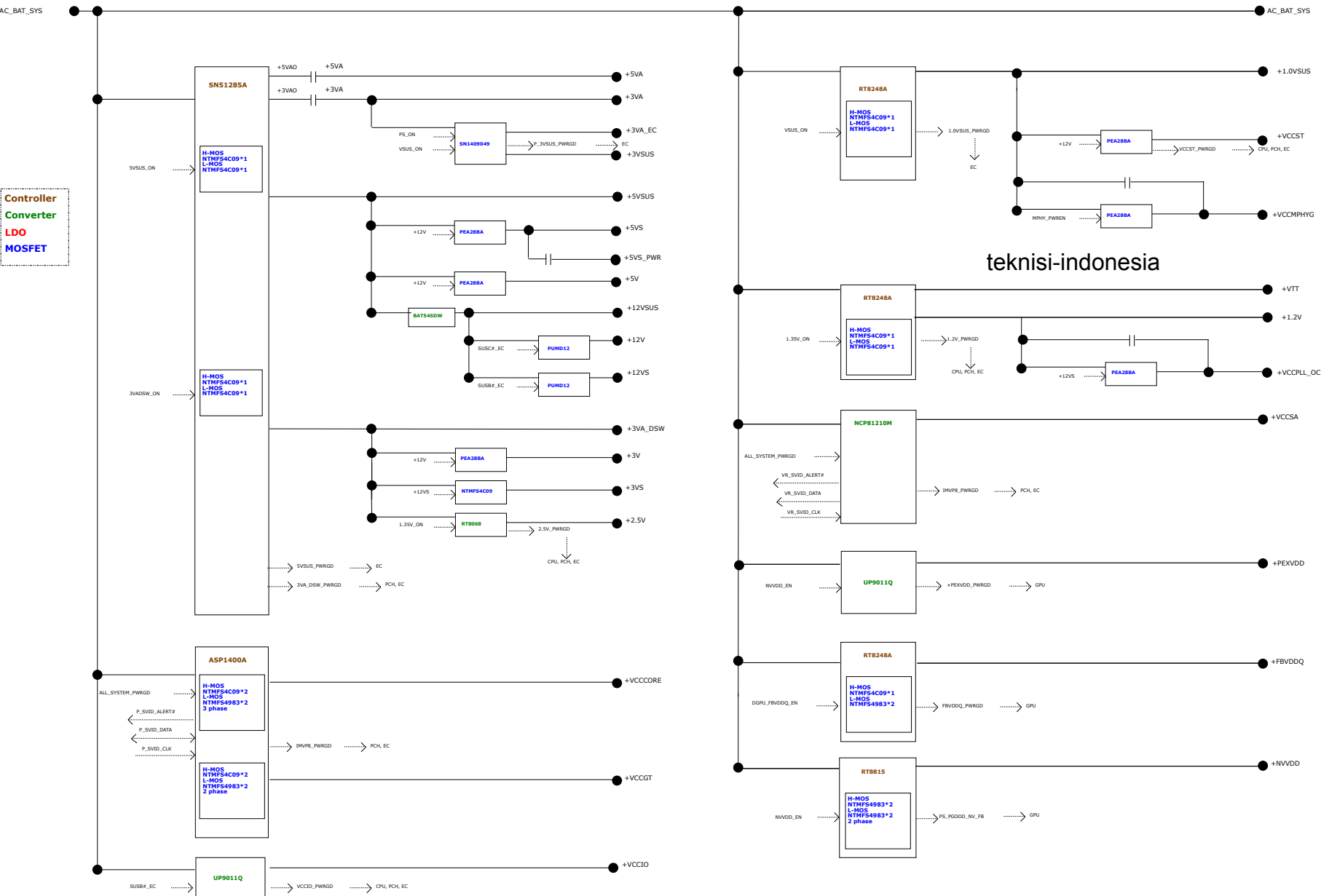
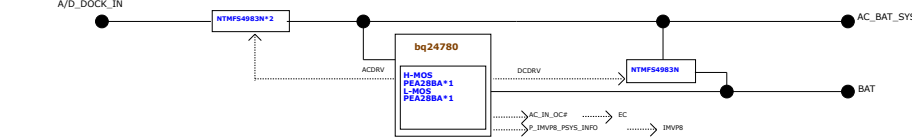
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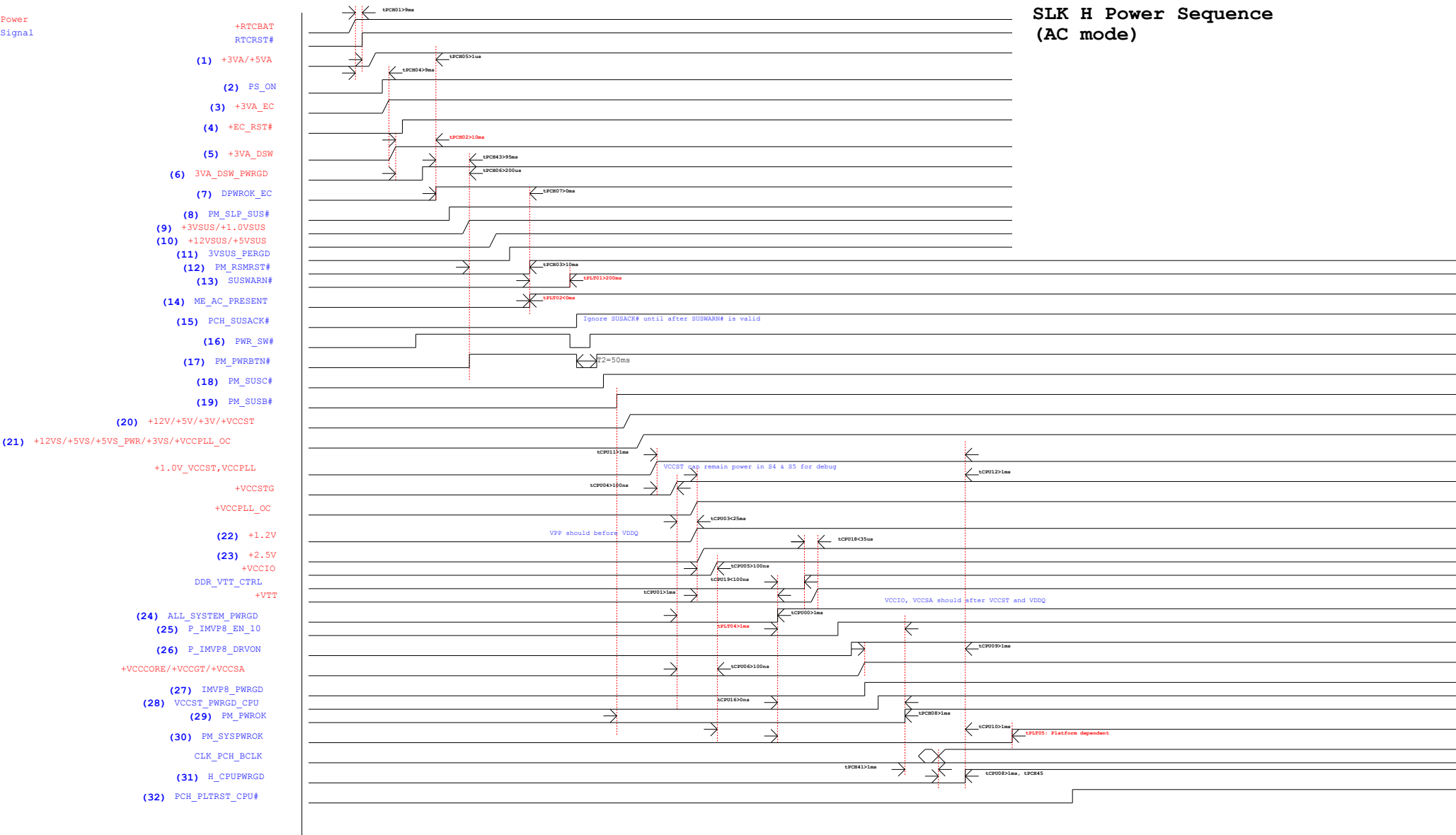
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of

103

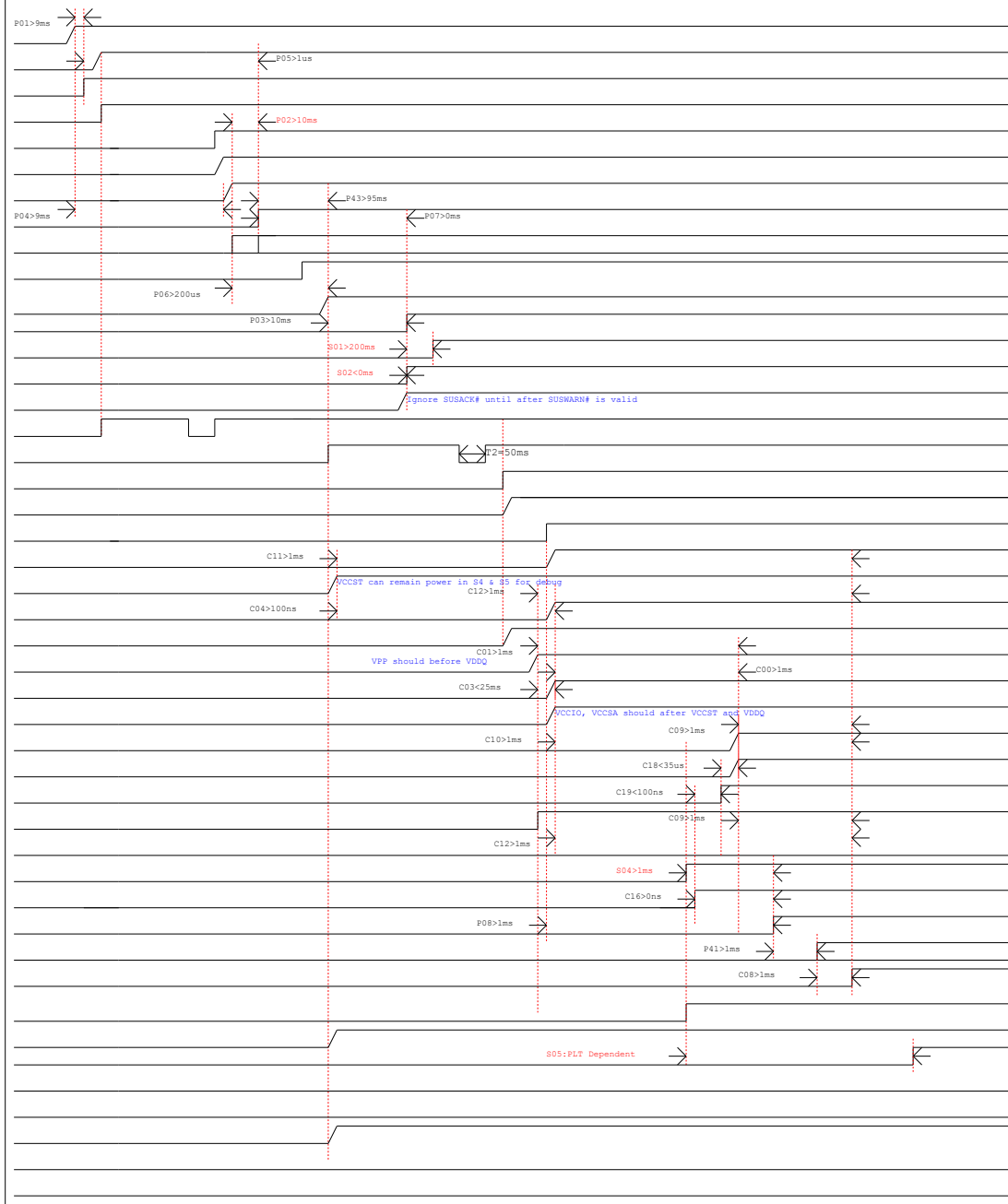


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Power
Signal

DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
P:PCH (AC_BAT_SYS)+3VA/+5VA
S:PLT (+3VA_RTC)RTCST#(PCH)
Power (Power)AC_IN_OC#(EC)
Signal (EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR_Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST,VCCPLL(VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPU_PWRGD(CPU)
(ALL_SYSTEM_PWRGD)P_IMVP8_EN_10(Power)
(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)
+VCCGT

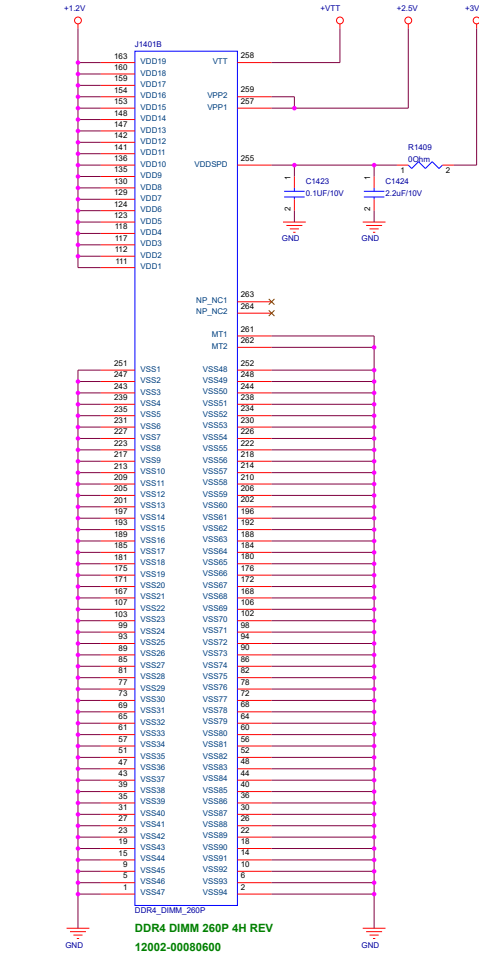


SLK H Power Sequence
(DC mode)

		Title : <u>Revision History</u>	
ASUS COMPUTER INC. HKT		Engineer: <u>Wenchi_Shen</u>	
Size 	Project Name GL552VXX		Ver. 2.0
Date: <u>Thursday, November 10, 2016</u>	Sheet <u>102</u> of <u>103</u>		

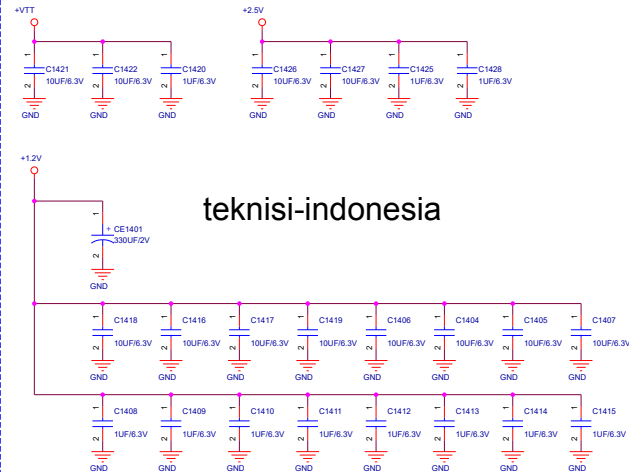
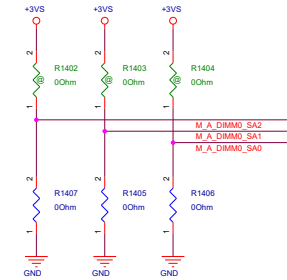


12002-00080600
DDR4 DIMM 260P 4H REV



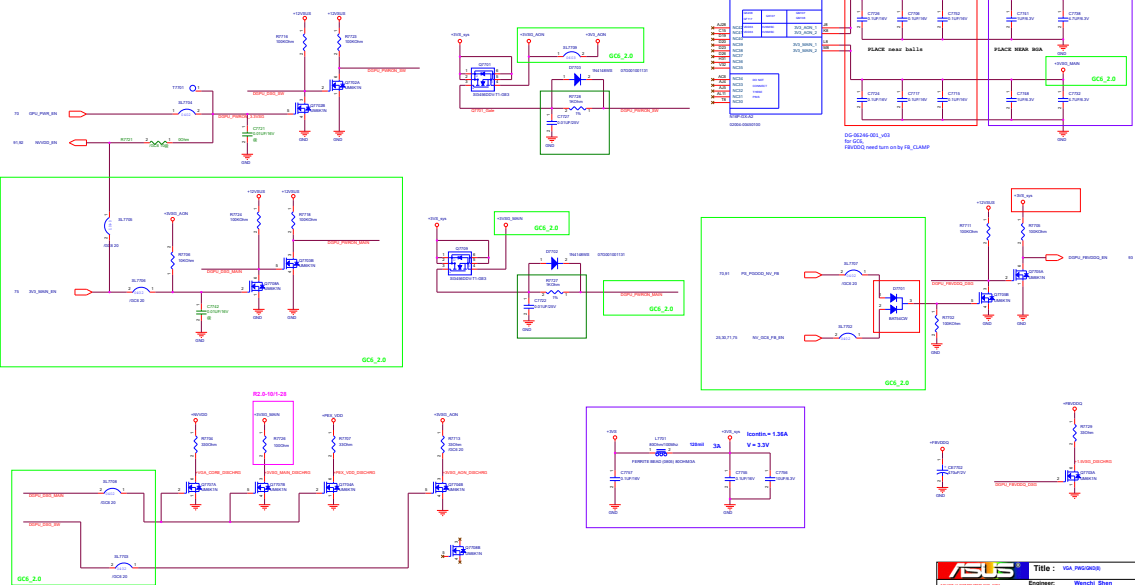
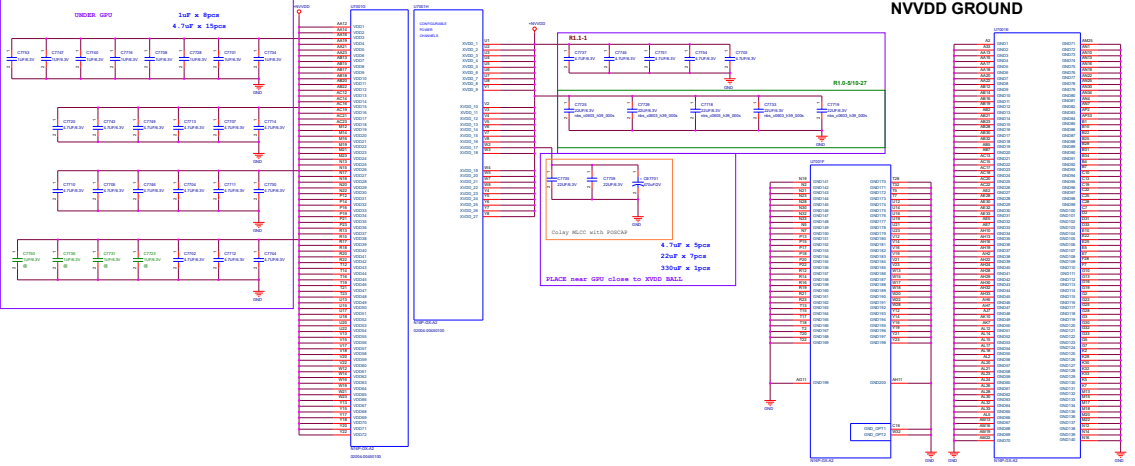
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired. SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

Schematic diagram of the R2.0-6/17-1 LED module. The module is a rectangular component with two pins. Pin 1 (left) is labeled '15.20' and 'DDR4_DRAMRST#'. Pin 2 (right) is labeled '15.30' and 'PM_EXTSTS#0'. The module contains an LED (D1401, VPORT0402L331V05, 07024-01170000) and a resistor (R1408, 200 Ohms). The LED is connected to Pin 1 and Pin 2. The resistor is connected to Pin 2 and ground (GND). The module is labeled 'R2.0-6/17-1'.



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NVVDD GROUND



Kabylake IMVP8 Power [For CPU]

